METRRA/FOLPES SIGNAL PROCESSOR AND SCAN CONVERTER

Goodyear Aerospace Corporation

Prepared for:

Army Mobility Equipment Research and Development Center

31 May 1974

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METRRA/FOLPES SIGNAL PROCESSOR AND SCAN CONVERTER FINAL REPORT

CONTRACT NO. DAAK02-73-C-0409

SUBMITTED TO

U.S. ARMY MOBILITY EQUIPMENT
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GERA-2002

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GOODYEAR AEROSPACE CORPORATION
ARIZONA DIVISION • • • LITCHFIELD PARK, ARIZONA

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ABSTRACT

This document is the final report on contractual effort performed on the METRRA/FOLPES Signal Processor and Scan Converter for the U.S. Army Mobility Equipment and Research Center, Fort Belvoir, Virginia, by Goodyear Aerospace Corporation, Litchfield Park, Arizona, under Contract No. DAAK02-73-C-0409. The objective of the effort was to design, develop, and fabricate hardware capable of processing coherent radar Metallic Reradiation Apparatus signals and displaying the resulting images on a standard color television monitor. The hardware is of a prototype nature and is usable under the Foliage Penetration System detection concept.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION I - INTRODUCTION

1. GENERAL

This document is the final report on U.S. Army Mobility Equipment Research and Development Center Contract DAAK02-73-C-0409 for METRRA/FOLPES Signal Processor and Image Display Component. The contractual effort was started in July 1973 and completed in May 1974. The objective of the effort was the design, development, and fabrication of hardware having the capability to process coherent radar Metallic Reradiation Apparatus (METRRA) signals and display the resulting image on a standard color television monitor. The hardware is of a prototype nature and is usable under the Foliage Penetration System (FOLPES) detection concept.

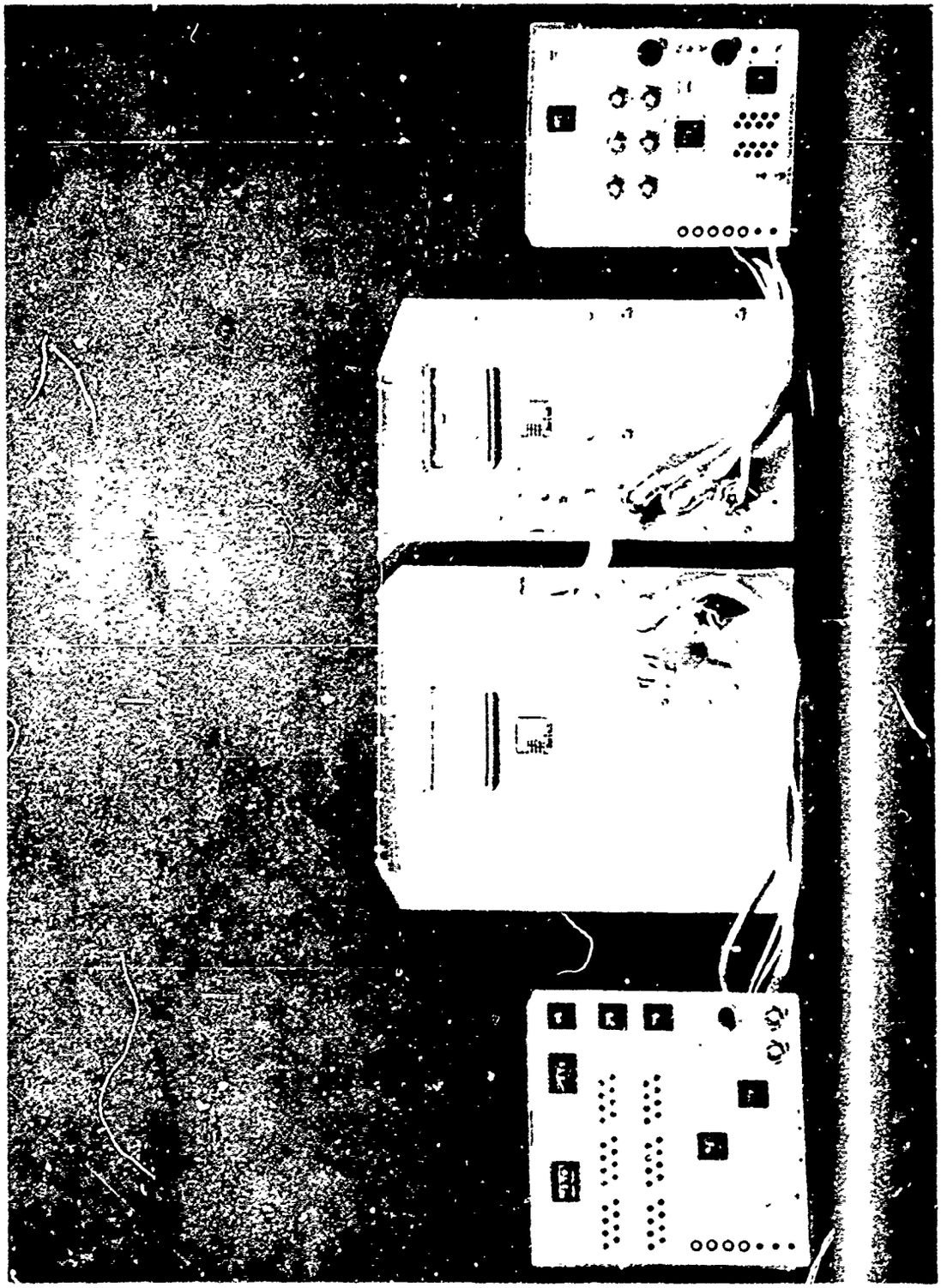
Figure 1 is a photograph of the equipment. On the left side of the photograph are the processor and processor control; on the right side are the scan converter and scan converter control. Interconnect wiring and power inputs are also shown. Inputs from the radar are accommodated by OSM type connectors, and outputs to the TV monitor are accommodated by BNC type connectors.

2. GENERAL REQUIREMENTS

The processor and scan converter were designed as physically separate units but compatible with each other in both configuratory and operational senses, so that they may work together as a unit (contract requirement). The devices were fabricated using the best available commercial practices for workable prototype equipment.

The equipment is capable of flight operation in an aircraft such as (or similar to) the Grumman "Mohawk" when due care is taken to reasonably assure laboratory environment (0 to 50 deg C at or below 3000 meters).

The equipment will operate either from 120 V, 60 Hz or from 28 VDC. The equipment will operate in any attitude. Physical characteristics and power requirements are shown in Table I.



4717-1

Figure 1 - METRRA/FOLPES Equipment

TABLE I - PHYSICAL CHARACTERISTICS AND POWER REQUIREMENTS

Equipment	Width (in.)	Height (in.)	Depth (in.)	Weight (lb)	Power
Processor	31	15-1/2	18	155	25.8 amps at 28 V
Processor control box	11-3/4	12	4-1/4	5	N/A
Scan converter	31	11	18	105	17.8 amps at 28 V
Scan converter control box	9-13/16	12	4-1/4	5	N/A

Maintenance of the units is facilitated by an inflight monitor and semiautomatic calibrator and tester. Two types of fault isolation are provided. First, a continuous monitor to all regulators is on each printed circuit board module, power supply, and subsystem module data clock. This monitor is in operation at all times and will indicate major failures at the printed circuit board level. A second type provides test signals to both the processor and scan converter so that known test patterns may be displayed on the color television monitor. In addition, signals are provided so that sidelobe levels, amplitude sensitivity, bandpass characteristics, and other system characteristics may be monitored at subsystem levels.

SECTION II - SYSTEM CONSIDERATIONS

1. GENERAL

The METRRA/FOLPES coherent radar system transmits a 100-nanosecond constant frequency pulse at a fixed PRF of 20 kHz with a 0.453-meter wavelength. Two parallel linear receivers operating at center frequencies of approximately 200 MHz and 600 MHz (1.36 and 0.453 meter wavelengths) provide input data to the fundamental and third harmonic coherent radar signal processors. The scan converter memory provides 192 range cells by 64 azimuth cells tor the fundamental image and 128 azimuth cells for the third harmonic image.

2. SYSTEM REQUIREMENT

The design specification of the radar signal processor is summarized in Table II.

TABLE II - DESIGN SPECIFICATION

Parameter	Value
Minimum range	0.1 km
Maximum range	9.9 km
Swath width	1.35 km
Range sample rate	10 MHz
Maximum aircraft velocity	250 knots
Minimum aircraft velocity	25 knots
Azimuth resolution	
Fundamental	3 deg
Third harmonic	1 deg

SECTION III - HARDWARE FUNCTIONAL DESCRIPTION

1. BASIC BLOCK DIAGRAM

a. General

This basic block diagram discussion will scan the block diagram and describe the control panels. More detailed discussions of each block are given in the following sections.

b. Processor

Figure 2 is the processor block diagram and Figure 3 is a photograph of the processor control panel. Separate A/D converters are provided for the in-phase and quadrature channels of the third harmonic data, but a single A/D converter is time shared on an every other radar pulse basis between the in-phase and quadrature channels of the fundamental data. This is possible due to the higher radar PRF and yields no processor degradation. The PRF buffer accepts the high data rate out of the A/D converters and utilizing the entire interpulse period dispenses the data at a much lower rate, thus allowing the processor to operate at a much reduced rate.

The azimuth processor provides the coherent doppler filtering (integration). It automatically compensates for aircraft velocity variations and adapts the filter bandwidth for different radar ranges (the filter bandwidth is fixed over the range swath, but changes as the center range changes). A manual override also allows the operator to select a desired filter bandwidth. The dynamic range of the azimuth processor is sufficient (24 bits) that even with the lowest aircraft velocity (25 knots) the processor has a low probability of overflow. The limit and roundoff circuit reduces the large processor dynamic range to eight bits. A control selects the position of the eight output bits relative to the input bits; i.e., it is a digital gain control.

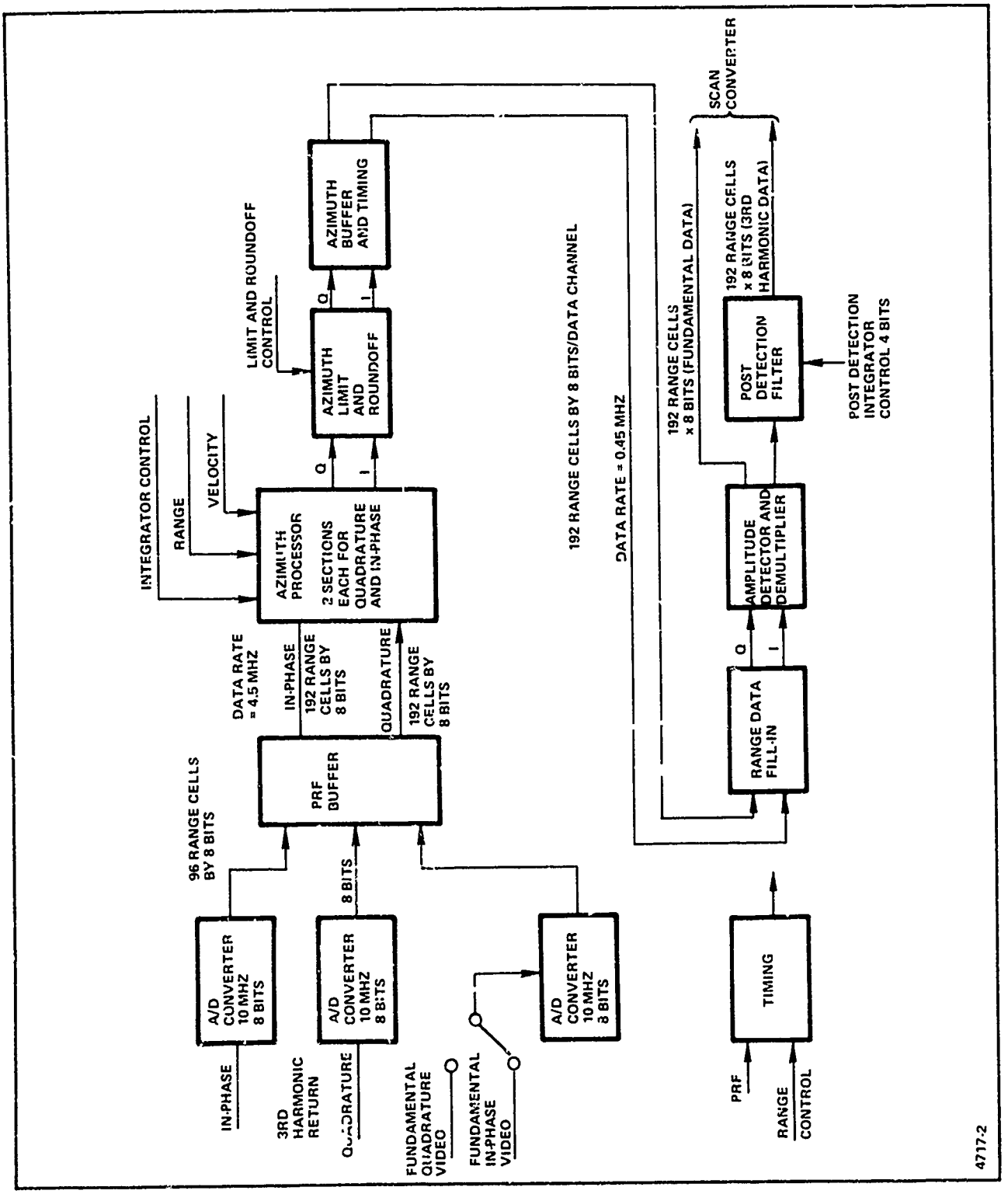


Figure 2 - Processor Block Diagram

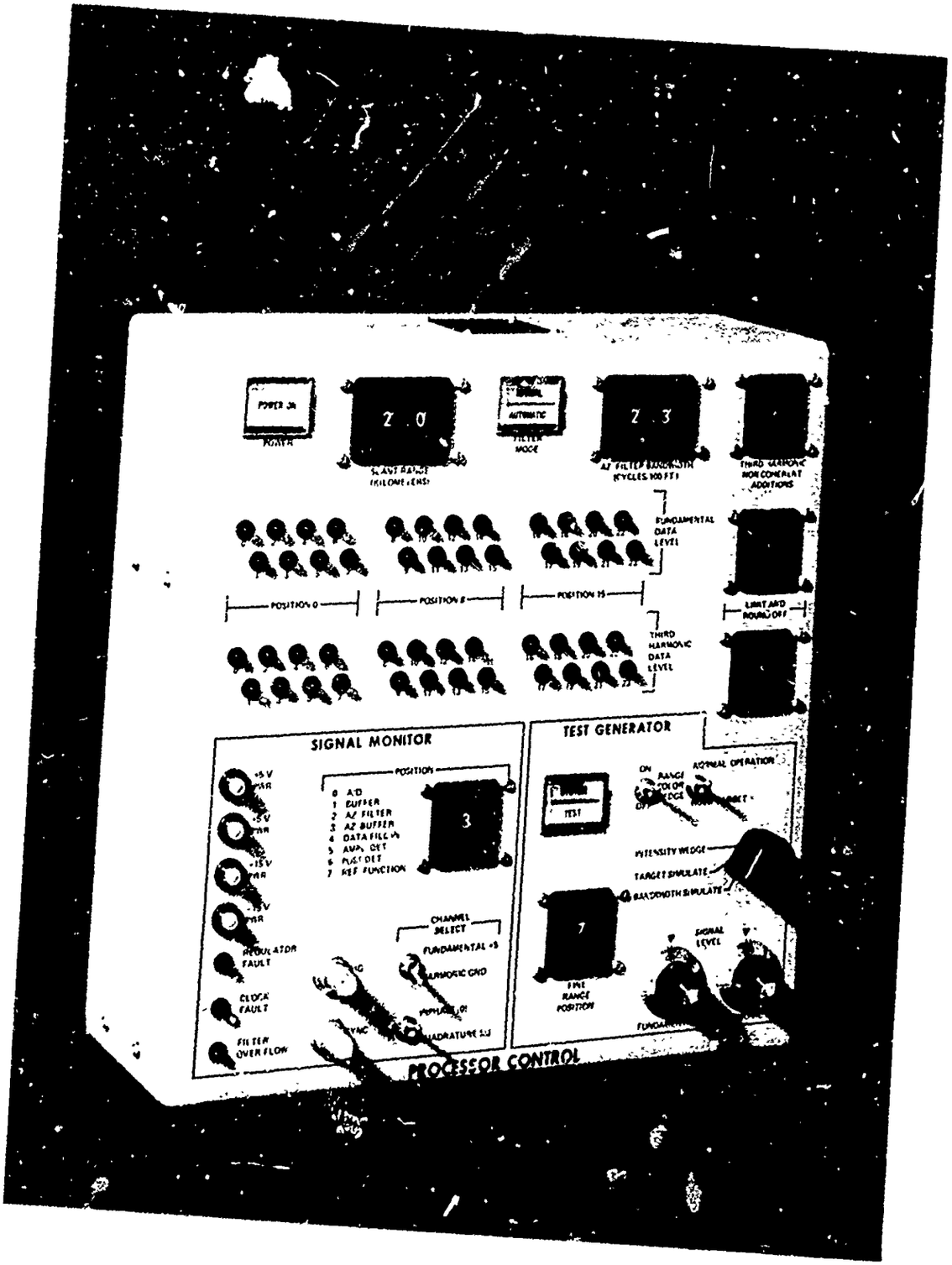


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Figure 3 - Processor Control Panel

The azimuth buffer further slows the data rate to the rest of the system. Range resampling doubles the sampling rate prior to amplitude detection where all phase information is destroyed. This provides the required sampling rate for the display and still allows the A/D converters and the processor to operate at half that rate. A detailed discussion of resampling is presented in Appendix A.

The amplitude detection determines the amplitude of the signal $\left|(I^2 + Q^2)\right|^{1/2}$ and no longer keeps the in-phase and quadrature data separate.

The postdetection filter (noncoherent integrator) on the third harmonic channel integrates P third harmonic outputs from the main processor. P is selected by the operator as one of the following: 1, 2, 4, 8, 16, 32, and 64. For example, if P is 8, then eight azimuth outputs from the main processor are added and the sum is sent to the scan converter. The resulting data rate to the scan converter is subsequently only one-eighth of that coming from the main processor. The total integration distance is held constant by varying the coherent processor integration length inversely with the postdetection filter. For example, if P = 1 and the coherent processor is integrating 4000 pulses and P is then switched to 8, the coherent integration would be automatically reduced to 500 pulses. This maintains constant sampling intervals going to the scan converter.

c. Scan Converter

A simplified block diagram of the scan converter is shown in Figure 4. The scan converter receives data from two azimuth processor channels and a third channel of color discriminator code data. An entire television frame of data is stored in the main memory of the scan converter, converted to an analog signal and supplied to the color television monitor.

Each azimuth processor channel periodically reads a new line of azimuth data into the scan converter. An updated azimuth line consists of 192 eight-bit words (each

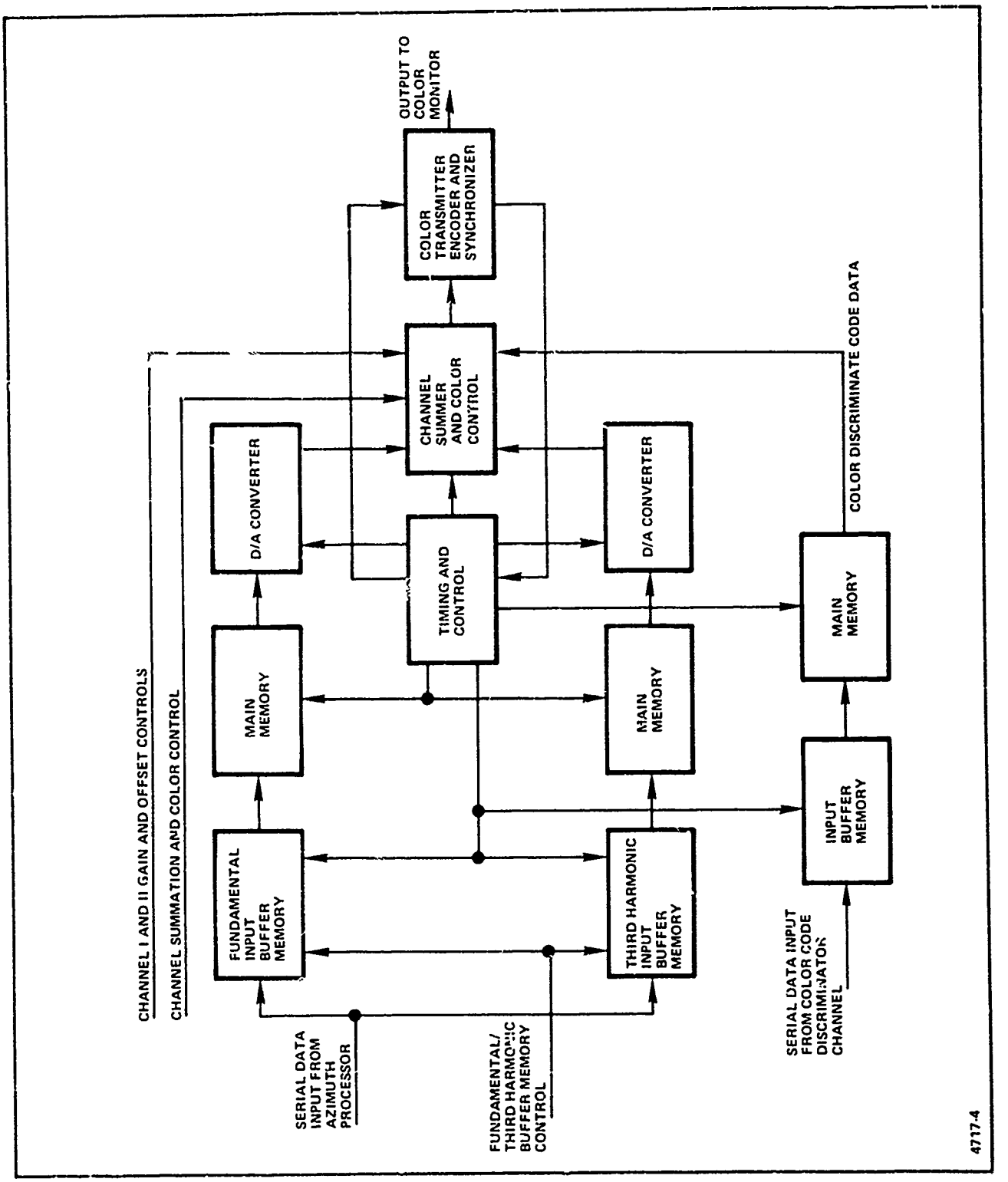


Figure 4 - Scan Converter Block Diagram

word representing a range element) for the fundamental processor, 192 eight-bit words for the third harmonic processor, and 192 three-bit words for the color channel.

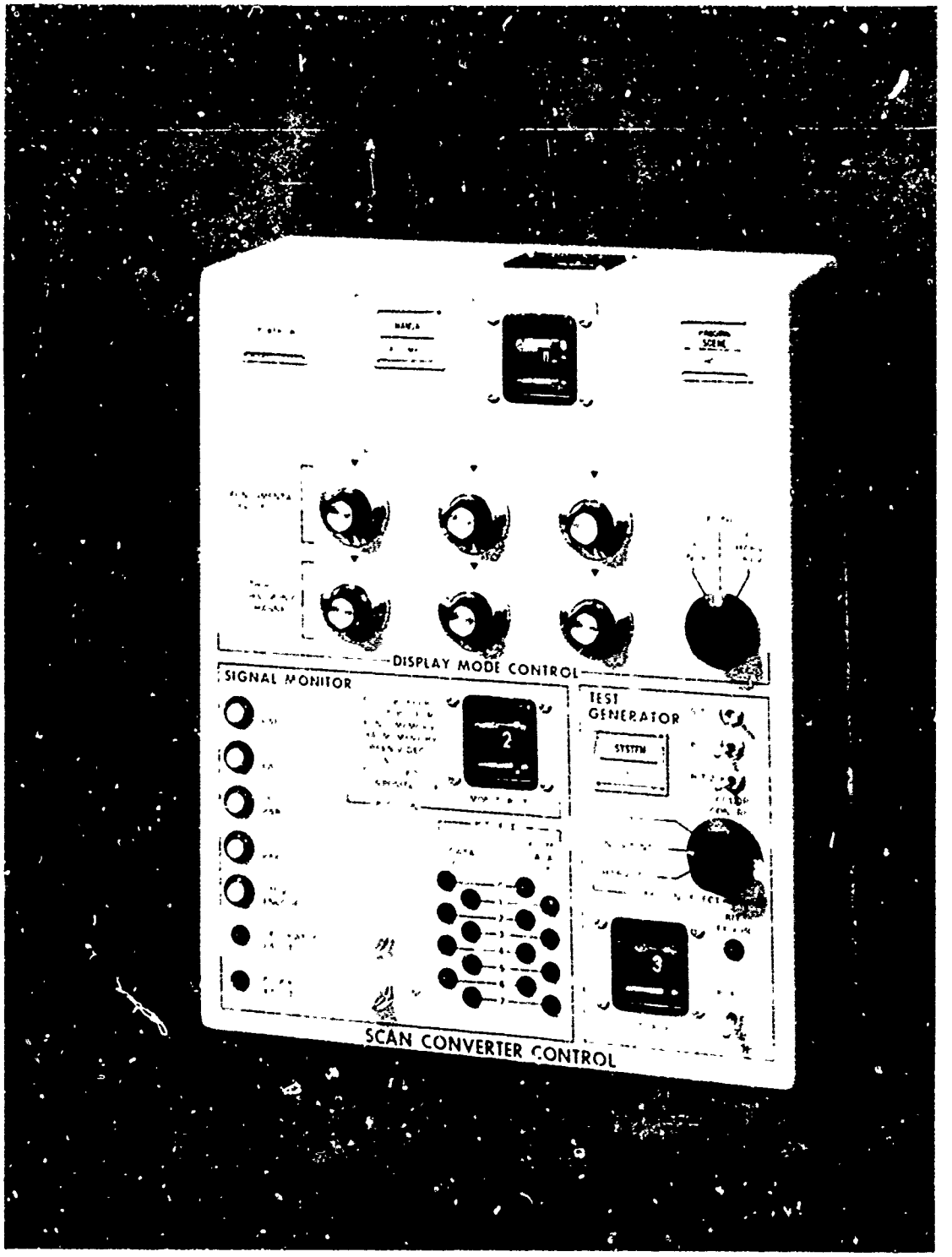
The fundamental and third harmonic processor outputs are received in a parallel format on separate lines together with a data clock and update synchronizing pulse. Because the azimuth update lines are received asynchronously with the main display memory timing, they are stored temporarily in an input buffer memory until the main display memory data has cycled to the proper position to accept the new data line. At this time the input buffer memory data is transferred into the main memory. The net effect is to produce a passing scene display on the monitor.

As stated earlier, the main memory stores one television frame of data and continuously refreshes the monitor's screen. During the one frame interval, all the data in each channel is scanned out and converted to an analog signal.

The timing which cycles the data stored in the main memory is synchronized with the timing sent to the television interface circuitry. Thus, the data and the television monitor are held in synchronism.

Controls are provided on the control panel to enable the operator to manipulate the display as desired (see Figure 5). A gain and offset control for each channel allows the operator to display all 256 gray levels or any portion thereof. Separate color and black and white controls are also provided for each data channel. This allows any amount of each channel to be displayed in color, black and white, or any combinations of their sums. The combined signal is then converted to the standard color television format by a color transmitter encoder and synchronizer.

One feature noted on the control panel allows the operator to choose between an automatic mode, which always maintains a 1-to-1 ratio between the display azimuth and range scale factors, and a manual mode allowing the operator to vary the range scale factor as desired.



4717-5

Figure 5 - Scan Converter Control Panel

2. PROCESSOR AND PROCESSOR CONTROL

a. Analog-to-Digital Converters

The A/D converters sample the video channels with a resolution of eight bits and a word rate of 10 megawords/second. Two A/D converters are used to sample the third harmonic channel - one for in-phase video and another for quadrature phase video. For the fundamental data channel, only one A/D converter is used. This single A/D converter is time shared between the in-phase and quadrature phase signal lines. This time sharing is on an every other pulse basis; i.e., on the odd-numbered radar pulses the in-phase data is digitized and processed and on the even-numbered pulses the quadrature data is processed. This time sharing scheme eliminates one A/D converter and one section of PRF buffer.

The A/D converter utilized is the CLB 0810 manufactured by Computer Labs. The selected A/D converter has 8-bit resolution and is capable of word rates from DC to 11 MHz. It also is small, operates over a temperature range of 0 deg C to 50 deg C, and uses system power supplies.

The timing to the A/D converter consists of a 10-MHz clock which is phase locked to a PRF synchronizing pulse from the radar. This synchronizing pulse must be coherent with the radar video. The clock is continuous except during the phase lock transition.

b. PRF Buffer

The PRF buffer receives 10 megaword/second data bursts of real-time radar data on the three channels[a] during the return swath time interval. This data is temporarily stored in memory banks composed of 32-bit random access memories, multiplexed onto two channels, in-phase and quadrature, and read out at a lower continuous

[a] Two of the channels are the third harmonic in-phase and quadrature data, and the third channel is alternately in-phase and quadrature data of the fundamental channel.

data rate. In this manner, the azimuth processor hardware is most efficiently utilized.

c. Azimuth Processor

The azimuth processor performs the following functions:

1. Shapes the azimuth spectrums for minimum sidelobe level
2. Determines the azimuth resolution of the processor.

The nonrecursive filter (finite impulse response) method was used to implement the azimuth processor. The nonrecursive filter method was selected on the basis of the accuracy of achieving the desired amplitude weighting, its versatility, and the amount of hardware required. The azimuth processor is effectively 192 separate filters, one for each range bin of both the fundamental and third harmonic channels. Even though the data shares the same hardware the data for a given range bin is never mixed with data from another range bin.

The basic concept of the finite impulse filter is to multiply the received data by a discrete reference function and add the results to the data from previous pulses in an accumulator, again keeping the data from each range bin separate. This continues each PRF until the azimuth synthetic aperture is completed. Then the accumulator is read out and the memory cleared ready to accumulate the range cells for the next synthetic aperture.

The azimuth processor consists of two basic parts: the filter section consisting of the multiplier and an accumulator, and the reference function generator.

Figure 6 shows a two-section finite impulse response filter for one data channel, either in-phase or quadrature. The other data channel is identical to the one shown.

The input format to the azimuth processor consists of 96 eight-bit range cells of fundamental data and 96 eight-bit range cells of third harmonic data. Each successive

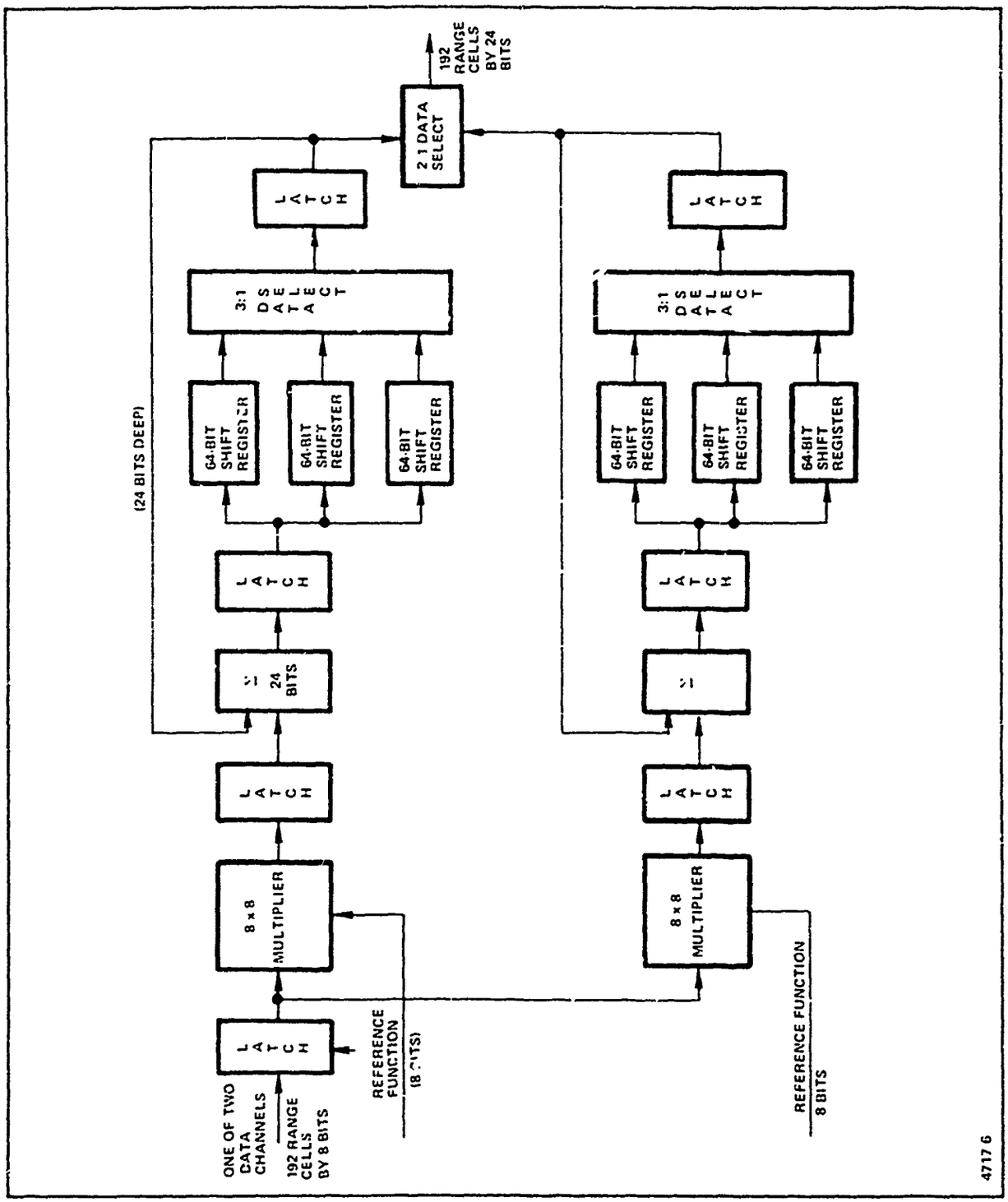


Figure 6 - Azimuth Processor Block Diagram for Either Quadrature or In-Phase Data Channel

range cell is latched and then multiplied with the eight-bit reference function. Each of the two multipliers have different eight-bit reference functions corresponding to the aperture weighting for that PRF. The reference function number remains fixed for the first 96 range cells, which represent the third harmonic data, and then is changed to a new reference function number for the second 96 range cells, which represent the fundamental data.

The 8 by 8 multiplier is capable of operating at a data rate of 7 MHz, which is well within the 4.75 MHz input data rate to the azimuth processor. The data output from each of the multipliers is sent to the accumulator. The accumulator is designed for 24-bit capability to accommodate successive additions of the 10-bit multiplier outputs over the synthetic aperture. The accumulator consists of a latch at the input to the 24-bit adder and latches at the output of the adder. The data is then multiplexed between three static 64-bit MOS shift registers in order to operate the MOS shift registers at an optimum data rate. Each accumulator section consists of 24-quad, 64-bit static MOS shift registers. The output of the shift register is demultiplexed by means of a 3 to 1 data select back to the input of the 24-bit adder, completing the accumulator cycle. A 2 to 1 data selector selects which filter is being read out.

The azimuth processor reference function generator provides the amplitude weighted reference functions as a function of velocity and range swath selection.

The azimuth processor reference function generator block diagram is shown in Figure 7.

The scaler generator receives the manually selected range swath and scales the range bits. The scaled range is multiplied by the velocity in a 10 by 8 multiplier. The output of the multiplier represents the distance traveled during a PRF interval. The output of the multiplier is accumulated in a 24-bit accumulator over the synthetic aperture length. An overflow from the accumulator signifies that the aircraft has flown a synthetic aperture length.

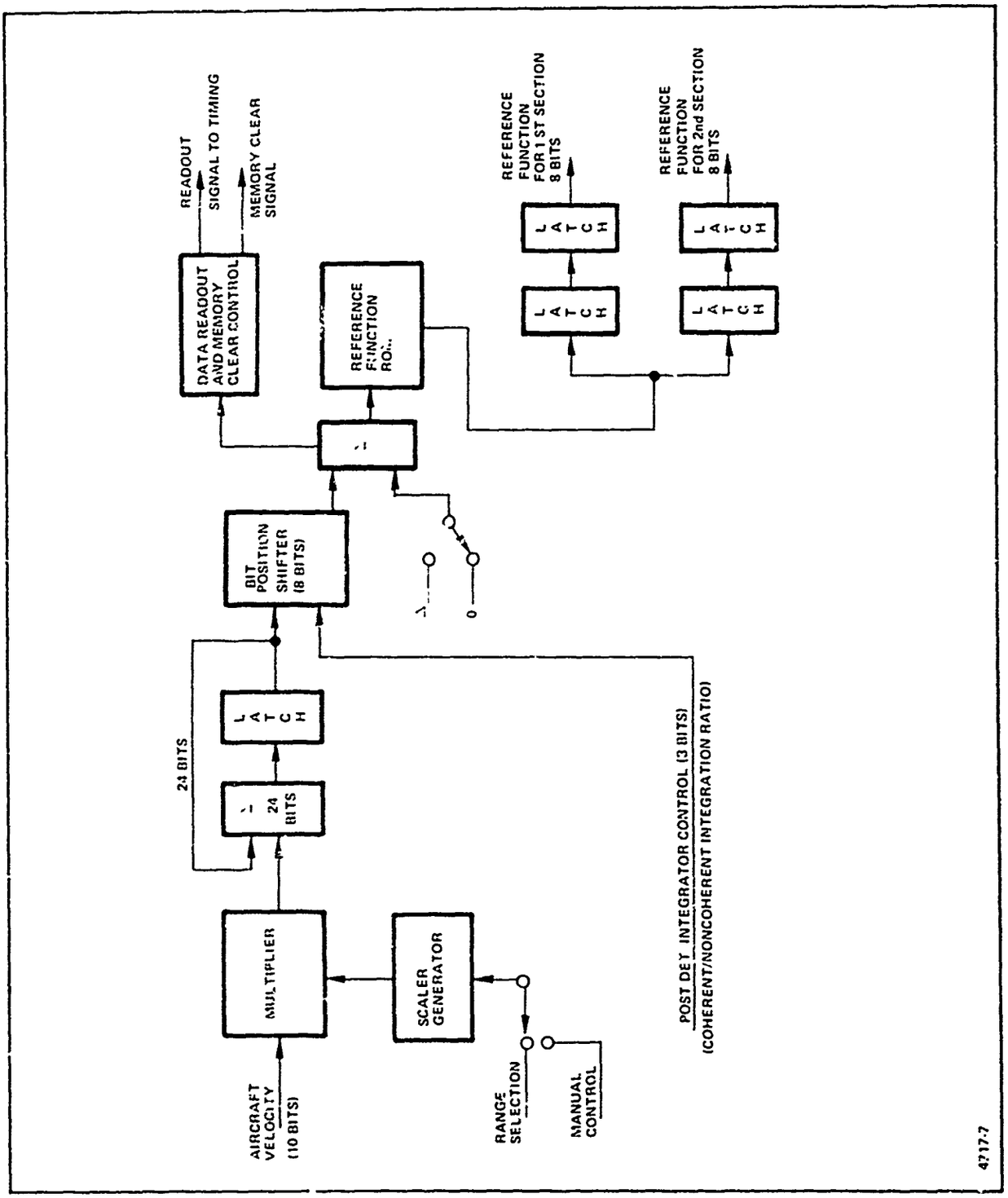


Figure 7 - Azimuth Processor Reference Function Block Diagram

An eight-bit position shifter accepts the accumulator data, which represent the distance moved across the synthetic aperture. The function of the position shifter is to shift the significance of the bits for the third harmonic reference as a function of the number of noncoherent integrations in the postdetection filter.

The output of the position scaler is summed with "Δ" and "0" alternately, which represent the reference offset between the two filter sections. The output of the adder is converted to the desired amplitude (cosine) weighting for minimum sidelobes by a programmable ROM (read only memory).

d. Azimuth Buffer

The purpose of the azimuth buffer and timing is to reduce the data rate in the same manner as was done in the PRF buffer. The data rate out of the azimuth processor is 4.75 MHz, but readout is approximately every thousandth PRF as a function of the synthetic aperture. Therefore, the data is buffered to reduce the data rate by approximately 10 to 1. The range cell data is multiplexed into three parallel 64-bit shift registers. Once the data is stored, it is read out of the shift registers with a much lower clock rate.

e. Range Resampling

The purpose of the range resampling is to increase the sampling rate of the range data prior to the detector to reduce spectrum overlap noise caused by the nonlinear nature of the detector (see Appendix A for rationale).

The range resampling circuits for the in-phase and quadrature channels are identical. A four-point approximation of a sine x/x function is applied to each data range cell for the in-phase and quadrature data channels. Each range cell is weighted by the function as follows: $-0.25\,Y_{n-2} + 0.75\,Y_{n-1} + 0.75\,Y_{n} - 0.25_{h+1}$, where Y is equal to the 8-bit range cell and n is time. The data is multiplied by means of a 2 to 1 data select which operates at twice the clock rate of the input data. The output

of the range resampling consists of a quadrature and in-phase data channel, each consisting of 384 eight-bit range cell data words (192 range cells of fundamental data and 192 range cells of third harmonic data).

f. Amplitude Detector

The amplitude detector calculates $(I^2 + Q^2)^{1/2}$ from the in-phase data channel and the quadrature data channel.

The eight-bit quadrature and in-phase data channels are squared by programmable ROM's and summed together.

The most significant four bits of the square root of the sum are obtained by an ROM.

The least significant four bits are determined by successive approximation. This unit is a standard board used on other processors.

g. Postdetection Filter

The postdetection filter provides noncoherent integration of segments of the synthetic aperture. A manual control allows the operator to select (in binary steps) from 1 to 64 noncoherent integrations per synthetic aperture. The 192 eight-bit range cell data words from the azimuth processor are stored in thirty-six (three in series by 12 deep) 64-bit static MOS shift registers. The stored data is subsequently summed, range cell for range cell, with the next processor output in a 16-bit adder and returned to the shift registers. After the desired number of accumulations, the data is routed to the scan converter and the shift registers are cleared. A limit and roundoff circuit reduces the possible 16-bit output to 8 bits for the scan converter.

To keep the data rate ratio constant between the third harmonic channel and the fundamental channel, the azimuth processor coherent integration length is varied inversely with the postdetection filter integration length.

h. Timing

The processor requires three different clock frequencies for operation.

The first clock is a phase locked oscillator which generates the 10 MHz A/D converter clock and read-in clock to the PRF buffer. The oscillator is phase locked to the transmitter waveform each PRF by means of the PRF synchronizer trigger. This ensures that the A/D converter sample clock is coherent with the in-phase and quadrature phase video return. The PRF buffer read-in clock is controlled by the manually selected range swath control to gate into the PRF buffer the desired video data from the A/D converters.

A second timing oscillator is used to read data out of the PRF buffer. This oscillator clock is also used in the azimuth processor, azimuth limit and roundoff, and the read-in clock to the azimuth buffer. This clock occurs during the time interval when data is not being read into the PRF buffer.

The third clock frequency provides the readout clock for the azimuth buffer, and the clock for the range data fill-in, amplitude detector, and postdetection filter.

3. SCAN CONVERTER AND SCAN CONVERTER CONTROL

a. Input Buffer Memory

The input buffer memory is capable of accepting input data at a maximum rate of 15,750 picture cells per second. The main display memory data is arranged so as to cycle four times each display frame of the color monitor. This allows the buffer memory access to the main memory once every 1/120 of a second. Therefore, the maximum number of input picture cells that are stored in the buffer memory is $15,750/120 \approx 132$.

The buffer memory is organized as shown in Figure 8. The block diagram represents one bit of storage. Because data can be received from both eight-bit image

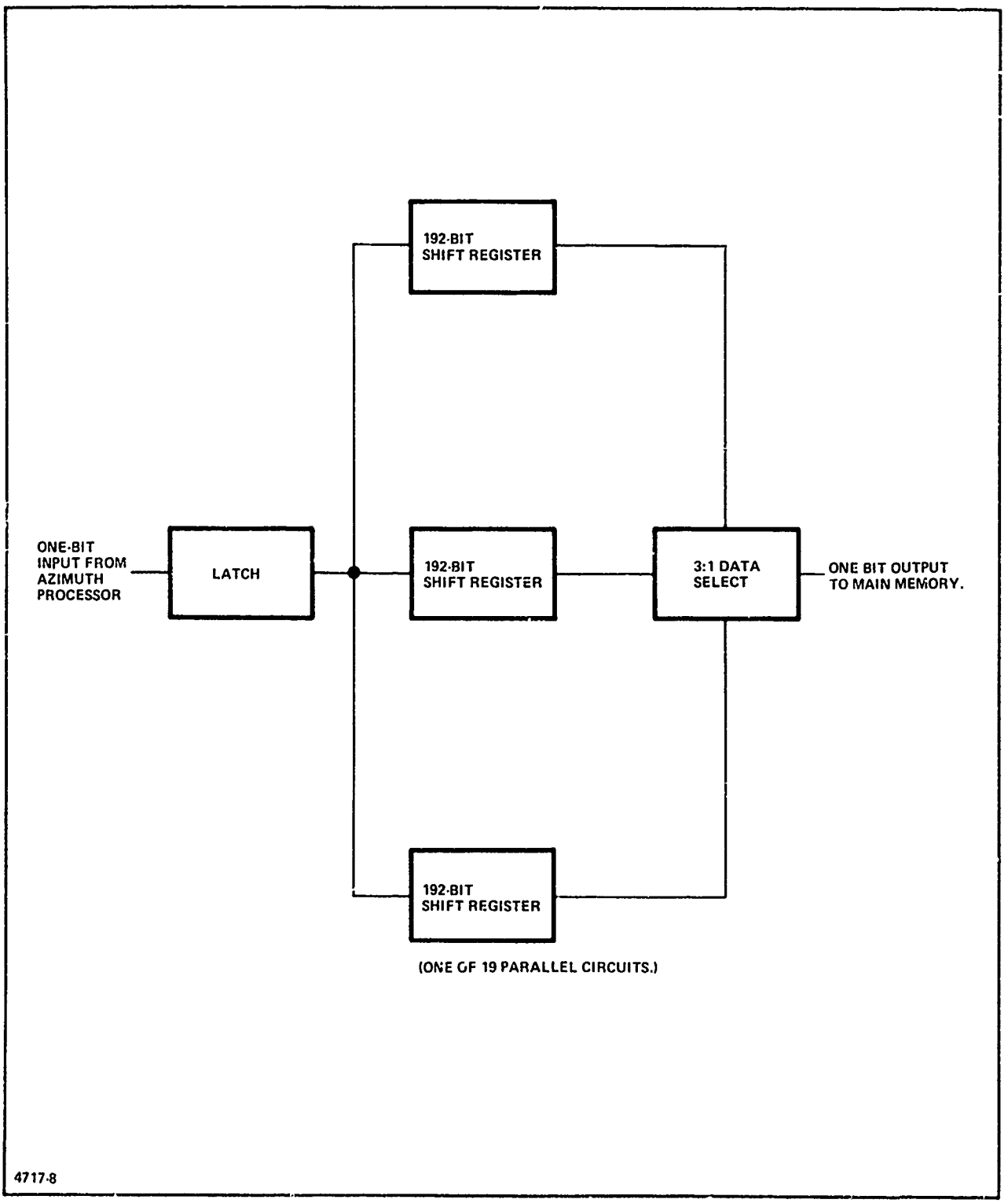


Figure 8 - Block Diagram of One Bit of the Scan Converter Input Buffer

channels as well as the three-bit color discriminate code simultaneously, the input buffer memory is composed of 19 of the circuits shown in Figure 8 arranged in parallel.

Three banks of buffer memories are arranged with common inputs. While one 192-bit buffer is accepting data, a second is at some stage of reading out, and a third is ready to receive new data in case the first memory fills before the second memory has finished reading out. In this manner the input buffer can accept a continual input data stream.

The required input buffer capacity is 10,944 bits. It is comprised of MOS shift registers and output selected through 3 to 1 data selects. The input buffer is packaged on one printed circuit card.

b. Main Display Memory

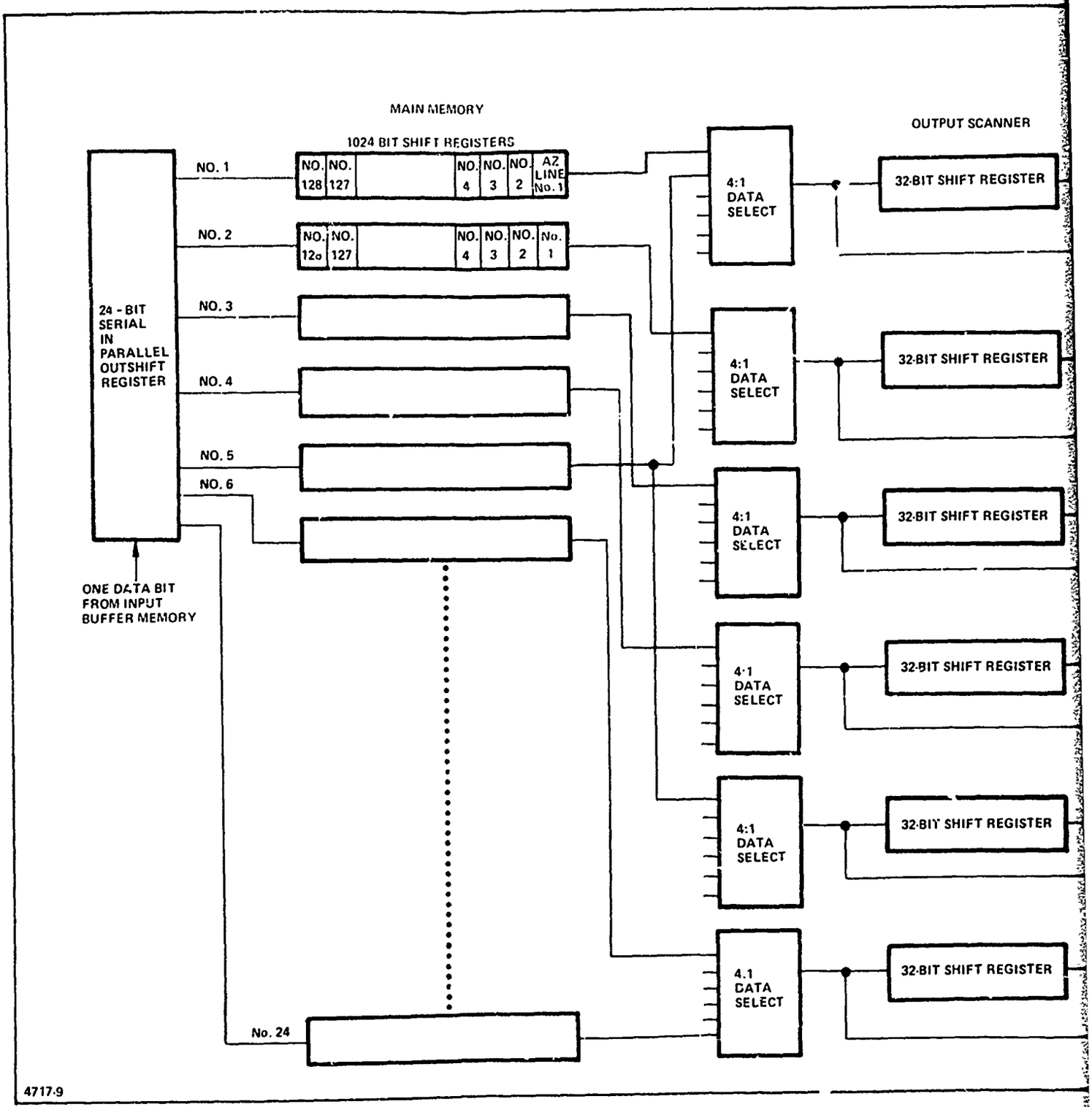
The main memory stores one television frame of data.

The third harmonic channel has the capacity of storing 128 azimuth lines, each with 192 cells for a total capacity of 196,608 bits (8 bits per cell). The fundamental channel has the capacity of storing 64 azimuth lines and 192 range cells for a total capacity of 98,304 bits. The color channel stores 128 lines and 192 range cells of color data for a total capacity of 73,728 bits. The total main memory capacity of the scan converter is 368,694 bits.

The main display memory receives data from the input buffer memory at a maximum rate of approximately 3 MHz. In the third harmonic and color discriminate code main memories, each bit is multiplexed by a factor of 24 and stored on 1024-bit shift registers. This allows the main memories to clock at a rate of approximately 125 kHz, which is well within the capabilities of high density MOS shift registers.

Figure 9 illustrates the data organization for one bit in the third harmonic and color discriminator code main memories. Each 1024-bit shift register contains data

from 8 range cells from each of the 128 azimuth lines. When 1 azimuth line is scanned out of the 24 shift registers, a total of 24 by 8 range cells are fed out. This represents the 192 range bins in a given azimuth line. The azimuth lines in the shift registers are arranged in the order 1, 2, 3,... 128. This organization is to accommodate the 525 standard television lines and also to reduce the required size of the input buffer memory by providing access to every cell in the main memory 120 times per second. To utilize the full television screen, each of the 128 azimuth lines of data would occupy four television lines, thereby filling 512 of the available television lines. The other 13 lines receive zero amplitude data and thus appear black. As line 1 data are read out, the data from the 24 shift registers are demultiplexed by a factor of six and then fed through more demultiplexing out to the D/A converters. The data is also stored in six 32-bit shift registers. On the second display line, the 1024-bit shift registers are not clocked and the 2-to-1 data selectors are switched to read out the data stored on the 32-bit shift registers. In this manner, line 1 is read out twice filling two television lines. Line 1 data fills another two television lines during the interlace. This process repeats 128 times until 1024-bit shift registers have completed 1 interlace cycle (1/60 second). During a television frame (1/30 second), the television monitor has scanned every other line (i.e., all the odd-numbered lines) for the first interlace (1/60 second). During the next 1/60 second (second interlace cycle), the monitor fills in the even-numbered lines with the same data as the odd-numbered lines. During this second interlace scan of the CRT, the memory again feeds out line 1 for two horizontal CRT display lines and repeats as described above. This organization reduces memory size and complexity to a minimum. By slightly modifying timing to the main memory board, the same board is used for the lower resolution fundamental processor channel; i.e., the memory boards for the fundamental and third harmonic are interchangeable.


MAIN MEMORY
1024 BIT SHIFT REGISTERS
OUTPUT SCANNER
24 - BIT SERIAL IN PARALLEL OUTSHIFT REGISTER
ONE DATA BIT FROM INPUT BUFFER MEMORY
NO. 1
NO. 2
NO. 3
NO. 4
NO. 5
NO. 6
No. 24
NO. 128
NO. 127
NO. 4
NO. 3
NO. 2
AZ LINE No. 1
No. 1
4:1 DATA SELECT
4.1 DATA SELECT
32-BIT SHIFT REGISTER
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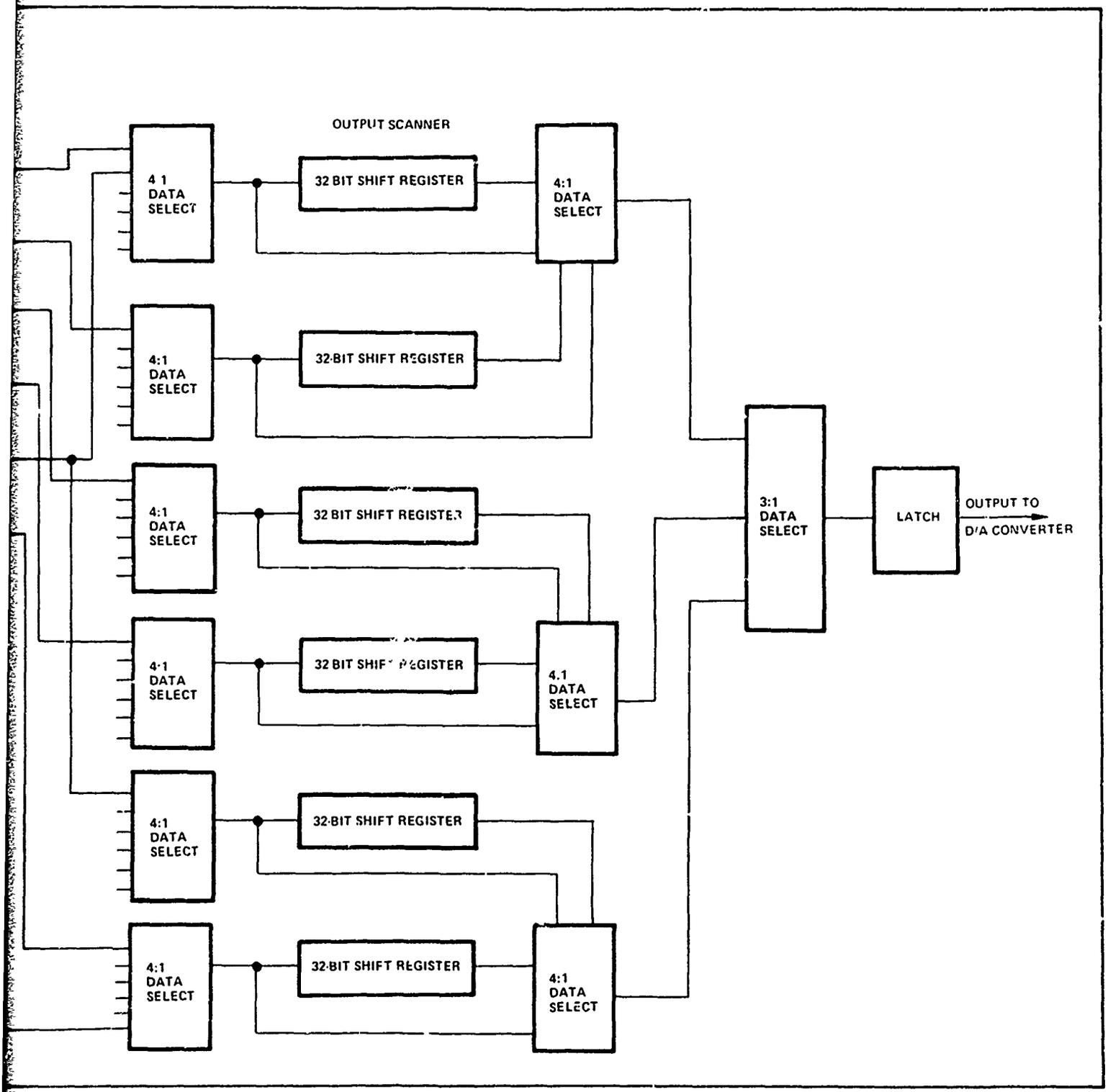


Figure 9 - Data Organization

B

c. Digital-to-Analog Converter

Eight-bit, 25-nanosecond settling time, D/A converters are used in the fundamental and third harmonic processor channels.

d. Channel Summer and Color Control Circuit

A block diagram of the circuit is shown in Figure 10.

The two analog data channels are applied to gain and offset control circuits. By varying the gain and offset controls (potentiometers located on the control panel), all or any portion of the 256 gray scale levels derived from the 8-bit A/D converters can be generated between an upper and a lower fixed voltage level as set by the limit and threshold control circuit. In this manner, the following summing amplifiers are never driven into saturation.

Each data channel is applied to two independent gain control circuits - a black and white gain control and a color gain control. As shown in Figure 10, the two black and white signals are summed together as are the two color signals. The summed black and white data are separated into blue, red, and green subchannels, each weighted by the proper fixed amount so as to convert it, after proper encoding, to a black and white signal on a standard color television monitor.

The summed color data is also separated into red, blue, and green subchannels which are weighted by variable gain controls as determined by the decoded color discriminator code signal. As a result, varying proportions of the two sums are displayed in color.

e. Color Transmitter Encoder and Synchronizer

The three color signals from the channel summer and color control circuit (representing blue, green, and red) are not directly adapted to a standard model color television monitor. A Telemation model TCE-2000 commercial color transmitter

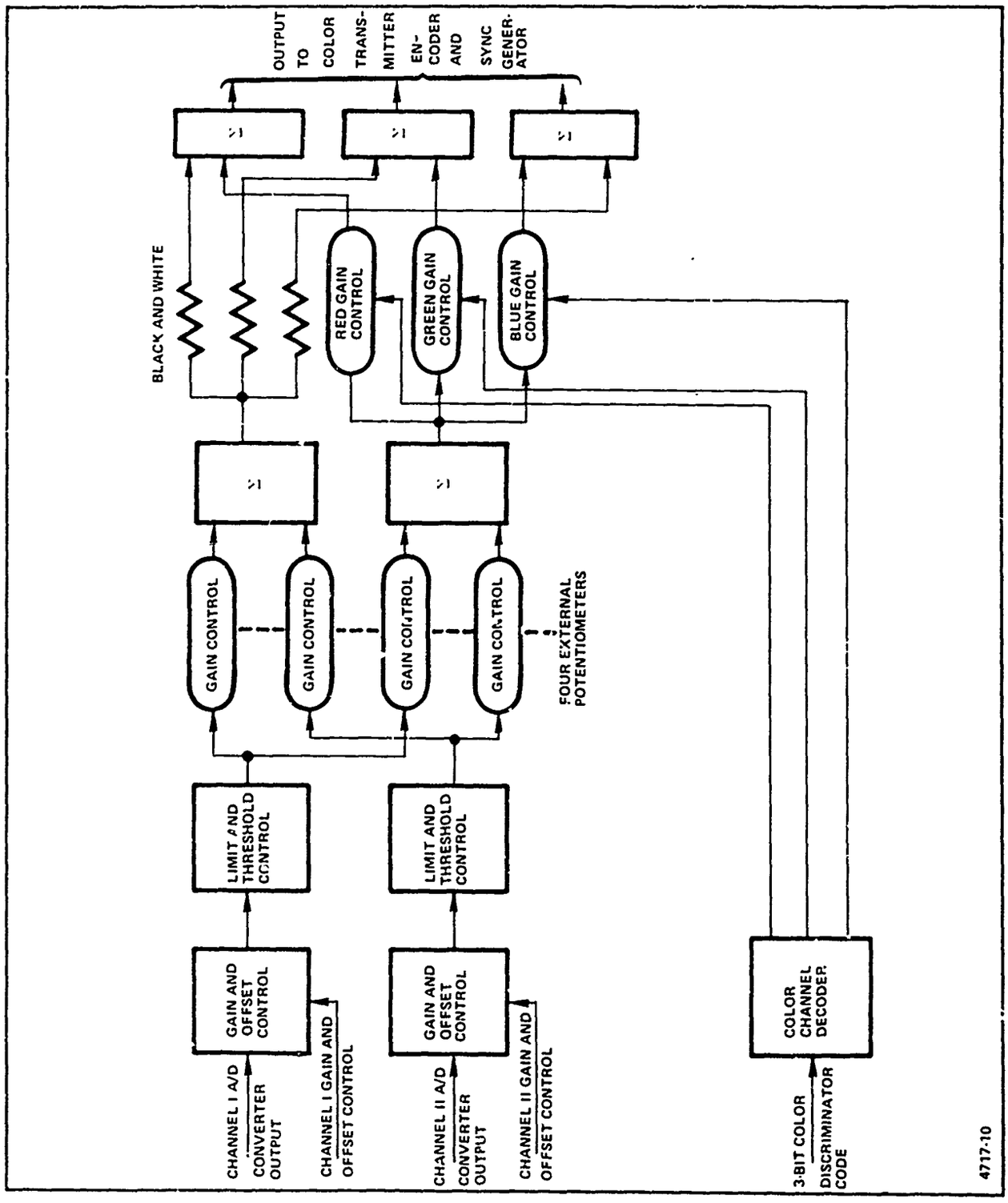


Figure 10 - Channel Summer and Color Control Detailed Block Diagram

encoder and synchronizer was interfaced with the scan converter output. This circuit generates the standard color television signal format consisting of in-phase and quadrature color channels superimposed on a luminance channel together with the synchronizing pulses and color bursts.

f. Timing and Control Circuit

The timing and control circuit provides the crystal control/clock and other timing signals used to synchronize the scan converter and the color monitor.

A control (see Figure 5) allows the operator to select between a mode in which the azimuth resolution and range resolution are identical and a mode in which the main memory clock is variable, thereby changing ratio between azimuth and range resolution as desired.

4. TESTER

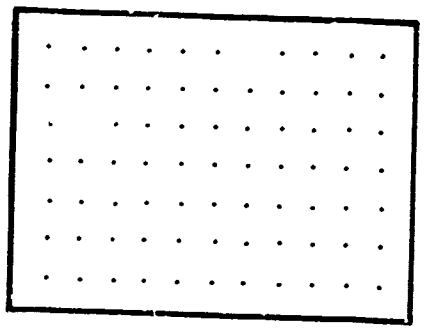
The tester provides a PRF pulse, two lines of analog video (in-phase and quadrature phase) signals, a 3-bit color number and a 10-bit velocity number. The two video lines are switchable between the fundamental and third harmonic channels. The video signals also have an amplitude control.

Three test signals generating three separate test patterns are available (see Figure 11):

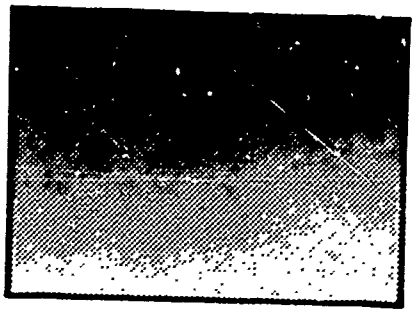
1. Target simulation. A simulated target is synthesized. It is gated so that every sixteenth range bin contains the target. The synthetic target generator recycles periodically, at a rate depending on velocity.

   The net pattern on the display is an array of dots which move across the display (passing scene).

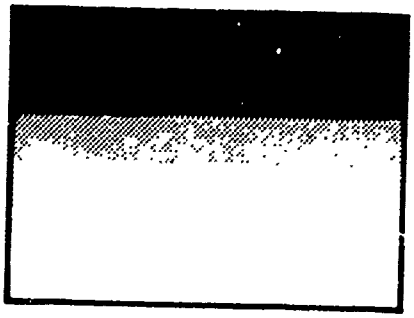
   The radar range of the simulated target is adjustable



(A) SIMULATED TARGET INPUT



(B) SWEPT FREQUENCY DATA



(C) INTENSITY WEDGE DATA

4717 11

Figure 11 - Expected Display Image for the Three Test Signals

2. Slowly swept doppler frequency. A sinusoidal doppler frequency signal is synthesized. Such a signal puts out a constant amplitude from the processor, the amplitude of which depends on the frequency. As the doppler frequency is changed, the display brightness represents the frequency spectrum of the azimuth filter. This test is very useful in determining if the least significant bits of the processor are working since the shape of the passband characteristics is quite sensitive while the synthetic target image is not

3. Stepped intensity wedge. A DC voltage is put onto the video lines and the level is periodically changed to a higher level. This puts an intensity wedge on the display. The size and frequency of the steps is selectable.

With each of these signals a color signal can be added. The color can be held constant or stepped in range (eight steps across the range swath). This stepped color yields a color wedge in the range direction. The range direction was selected so that it would be orthogonal to the intensity wedge which is in the azimuth direction.

5. FAULT ISOLATION DEVICE

The monitor for regulators on printed circuit cards consists of monitor wires from each of the regulators. The output of each regulator is sequenced and compared with an upper and lower voltage limit. If a regulator is not within the preset limits, an indicator light on the control panel so indicates. On the monitor board, indicator lights which represent each of the card regulators are provided to show the exact location of the failure.

Indicator lights are also provided for the scan converter and processor power supplies. The data clock monitor monitors the data clocks at the submodule level with the use of monostables which detect the absence of the clock. The output of the data and indicator lights on the control panel indicates failure of any of the module data clocks.

The data output of the scan converter is monitored for the fundamental and third harmonic channels. Two sets of eight lights, which represent the bit level of each channel, are provided on the control panel. The indicator lights provide a coarse indication of the data sensitivity.

Each of the data outputs from all subsystem modules is selected from a switch on the control panel to monitor any eight-bit data channels. The selected data channel is converted to an analog signal for ease of observing the waveforms by means of a fast eight-bit D/A converter. A trigger is also provided which corresponds to each of the selected data channels. Test jacks are provided for the analog data and trigger for observation on an oscilloscope.

The test points for the eight-bit digital data are also provided for direct observation of the digital data

Data selects are provided on the output of the following submodules for monitoring:

1. Three A/D converters
2. PRF buffer
3. Azimuth filter
4. Azimuth limit and roundoff
5. Azimuth buffer
6. Range data fill-in
7. Amplitude detector
8. Postdetection filter
9. Scan converter buffer memory
10. Scan converter main memory.

SECTION IV - HARDWARE PHYSICAL DESCRIPTION

1. GENERAL

This section summarizes the physical characteristics of the METRRA/FOLPES processor and scan converter.

2. PROCESSOR

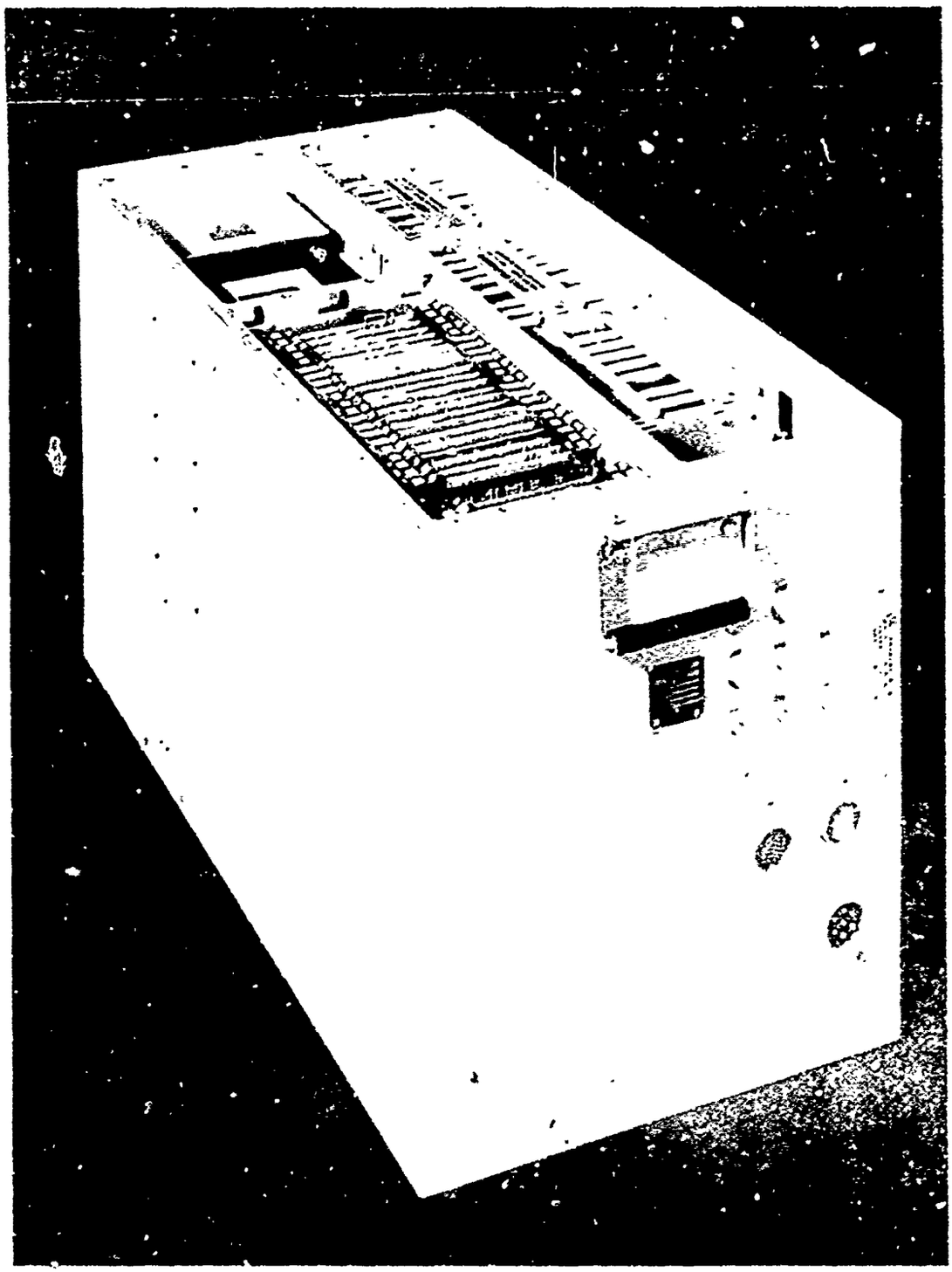
Figure 12 is a photograph of the processor with the top cover removed to show the arrangement of the major components. The card rack and two power supplies are shown on the left-hand side. The three A/D converters are shown on the right-hand side. There are 26 slots in the card rack of which 23 are used. Figure 13 is a view of the bottom of the processor with the bottom panel removed. Three cooling fans not shown are attached to the bottom panel. The lower part of the photograph shows the three A/D converters. The back plane wiring of the card rack is shown in the upper part of the photograph.

The functional description and physical position of the 23 printed circuit boards are shown in Table III.

3. SCAN CONVERTER

Figure 14 is a photograph of the scan converter with the top cover removed to show the color encoder, card rack, and one of the required power supplies. The scan converter card rack can also accommodate 26 printed circuit cards; however, only 20 cards are required. The organization of the memory will permit expansion in the along-track direction. Figure 15 is a view of the bottom of the scan converter with the bottom panel removed. Three cooling fans are also mounted on the bottom panel of the scan converter

The physical position and functional description of the 20 printed circuit boards of the scan converter are shown in Table IV.



4717-18

Figure 12 - Top View of METRRA/FOLPES Processor

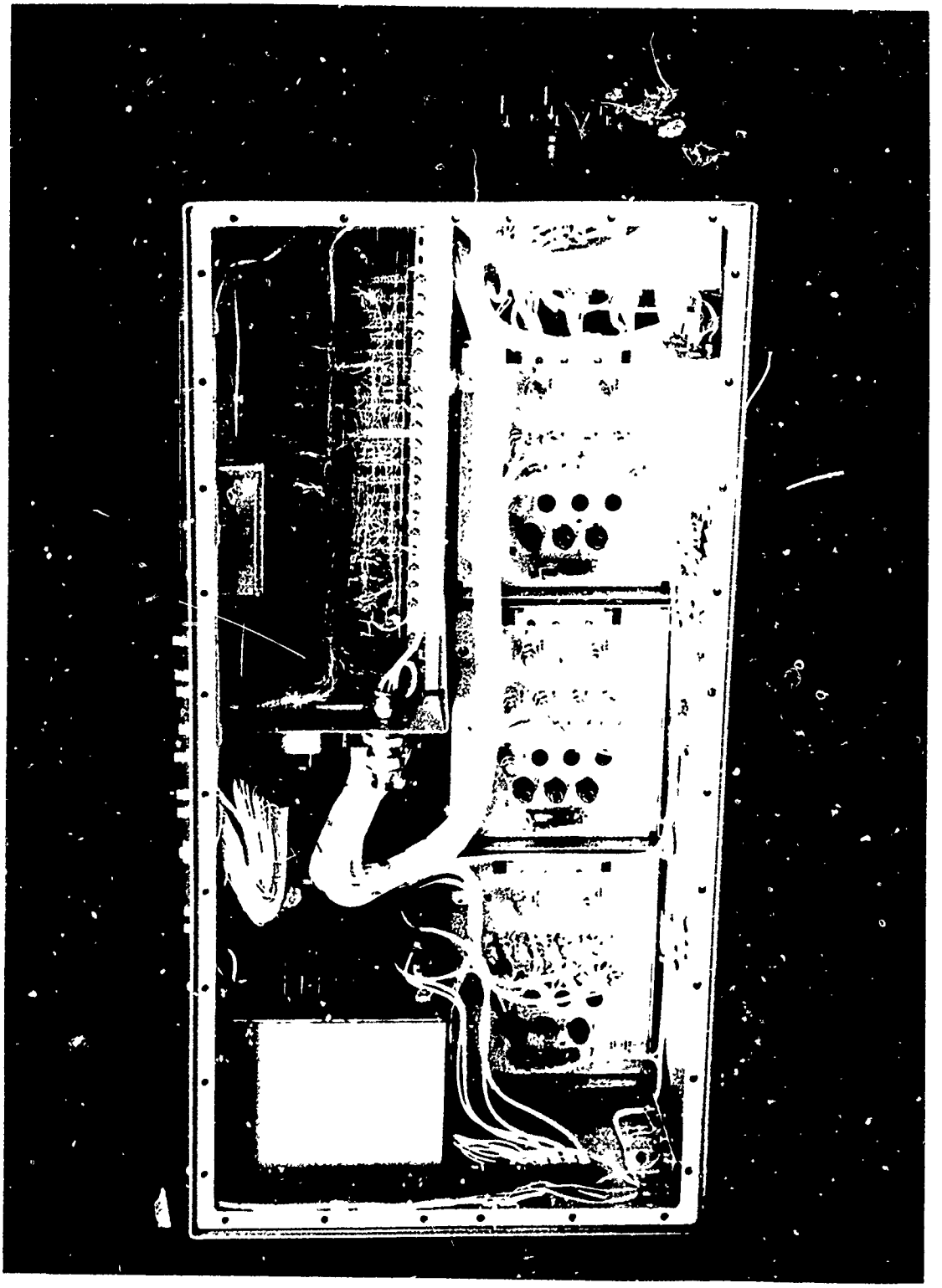
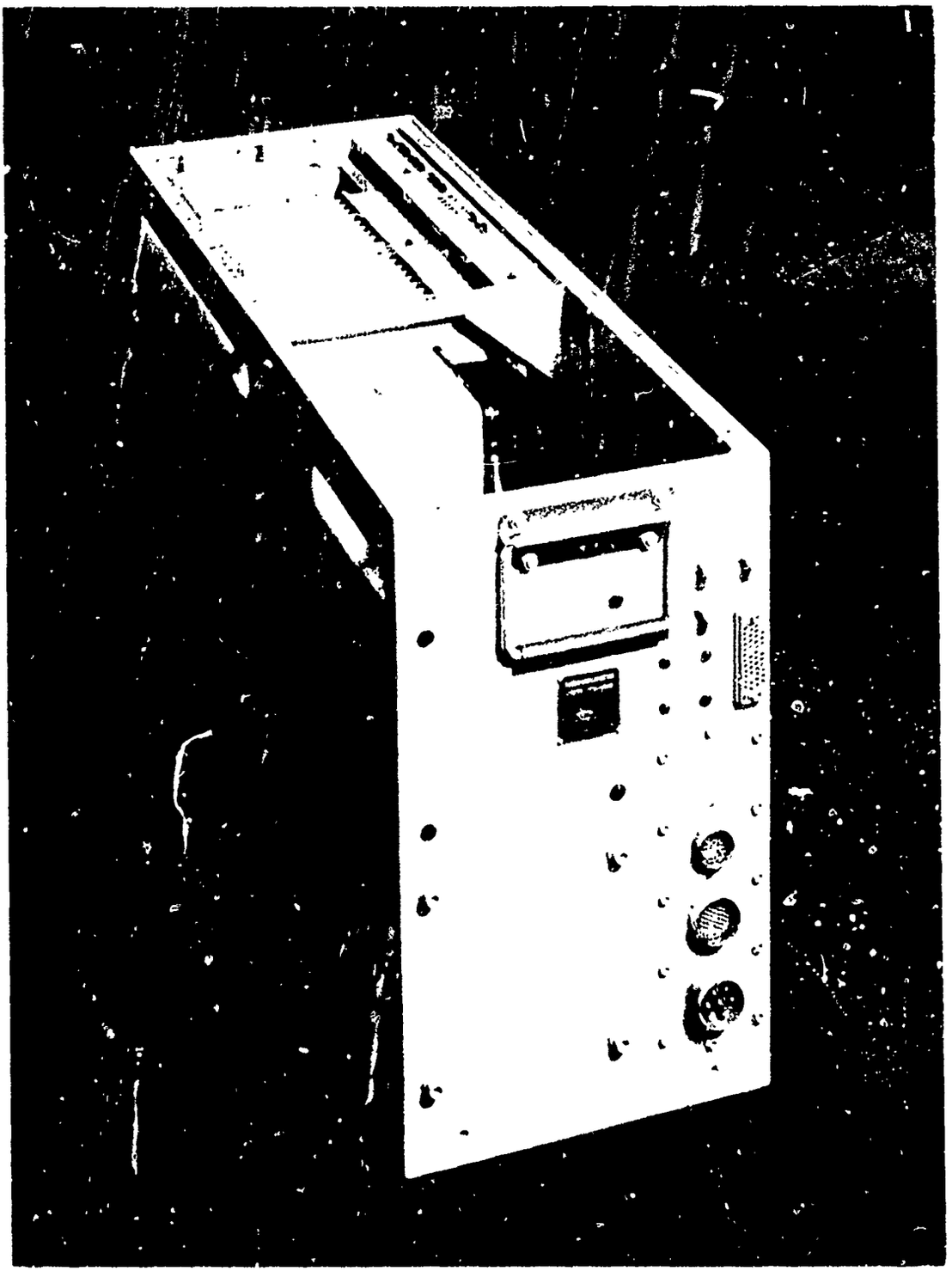


Figure 13 - Bottom View of METRRA/FOLPES Processor

4717-19

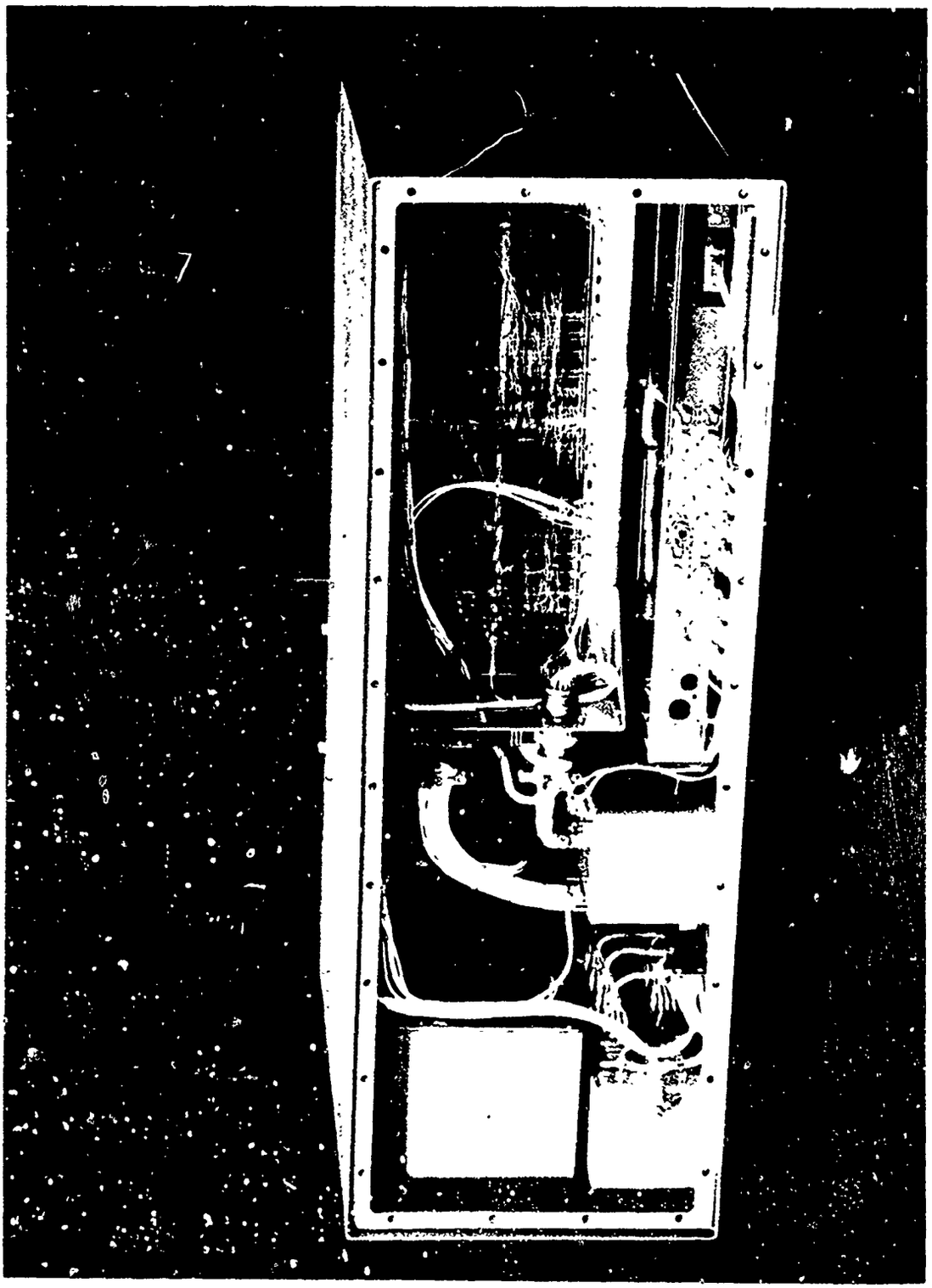
TABLE III - PRINTED CIRCUIT BOARDS

Position	Functional description
J2	Regulator monitor
J3	Signal monitor
J6	Post detection
J7	Amplitude detection
J8	Range data fill-in
J9	Azimuth buffer
J10	Azimuth limit and roundoff no. 2
J11	Azimuth filter circuit no. 2
J12	Azimuth filter circuit no. 1
J13	Azimuth filter circuit no. 2
J14	Azimuth filter circuit no. 1
J15	Azimuth reference function circuit no. 2
J16	Azimuth reference function circuit no. 1
J17	Azimuth limit and roundoff no. 1
J18	Azimuth filter circuit no. 2
J19	Azimuth filter circuit no. 1
J20	Azimuth filter circuit no. 2
J21	Azimuth filter circuit no. 1
J22	PRF buffer (third harmonic)
J23	PRF buffer (fundamental)
J24	Processor timing
J25	Tester no. 2
J26	Tester no. 1



4717-20

Figure 14 - Top View of Scan Converter



4717-21

Figure 15 - Bottom View of Scan Converter

TABLE IV - SCAN CONVERTER PRINTED CIRCUIT BOARDS

Position	Functional description
J1	Color combiner and control
J2	Regulator monitor
J8	Main memory (harmonic)
J9	Main memory (harmonic)
J10	Main memory (harmonic)
J11	Main memory (harmonic)
J12	Harmonic buffer memory
J13	Harmonic and color timing and control
J14	Color buffer memory
J15	Main memory (color)
J16	Main memory (color)
J18	Data monitor
J19	Main memory (fundamental)
J20	Main memory (fundamental)
J21	Main memory (fundamental)
J22	Main memory (fundamental)
J23	Fundamental buffer memory
J24	Fundamental timing and control
J25	Clock generator
J26	Main timing

APPENDIX A -

PROCESSOR SAMPLING RATE AND RESAMPLING

1. WHY RESAMPLING IS USED

The size, weight, power consumption, and consequently the cost of a digital processor are directly proportional to the data rate or sampling rate. For this reason any technique which minimizes the sampling rate is utilized in the processor design. To process for a given resolution, according to the Nyquist sampling theorem, the minimum sampling rate must be approximately two samples per resolvable element.[a] In a two-channel (in-phase and quadrature phase) processor, the bandwidth and consequently sampling rate in each channel is reduced by a factor of two, but the overall bandwidth remains constant. When the two channels are combined into a single channel (i.e., converted to a magnitude signal) by passing through a nonlinear detector, the resultant bandwidth is approximately equal to the sum of the in-phase and quadrature phase channel bandwidth.[b] This is shown in Figure A-1(A). As a result, according to the Nyquist sampling theorem, the sampling rate through the detector must be doubled to separate the signal spectrum from the unwanted aliased spectrum caused by sampling. This is illustrated in Figure A-1(B).

If a nominal amount of distortion can be tolerated, the detector sampling rate can be less than twice the processor sampling rate. However, as can be seen in Figure A-1(C) and (D), the spectra begin to overlap. Drawings illustrating the display responses for the detector sampling rates illustrated in Figure A-1(B), (C), and (D) are shown in Figures A-2, A-3, and A-4, respectively. As can be seen, a tradeoff exists between display resolution and sampling rate.

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[a] The sampling rate must be slightly higher to process for lower sidelobes.

[b] Lawson and Uhlenbeck: Threshold Signals, Radiation Laboratory Series. New York, New York, McGraw-Hill Book Co., Inc., 1950, pp. 62-63.

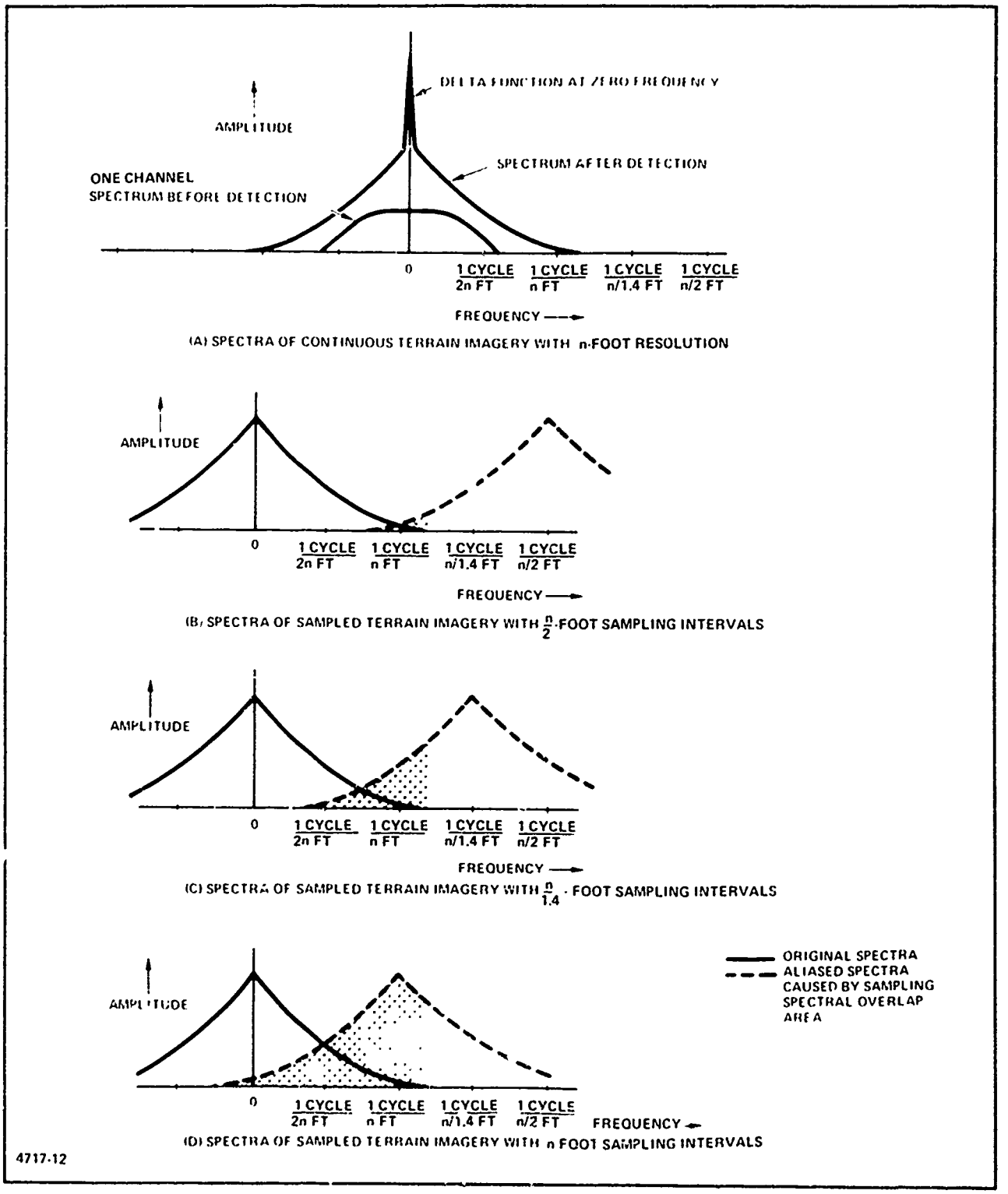

Figure A-1 - Processor Data Spectra

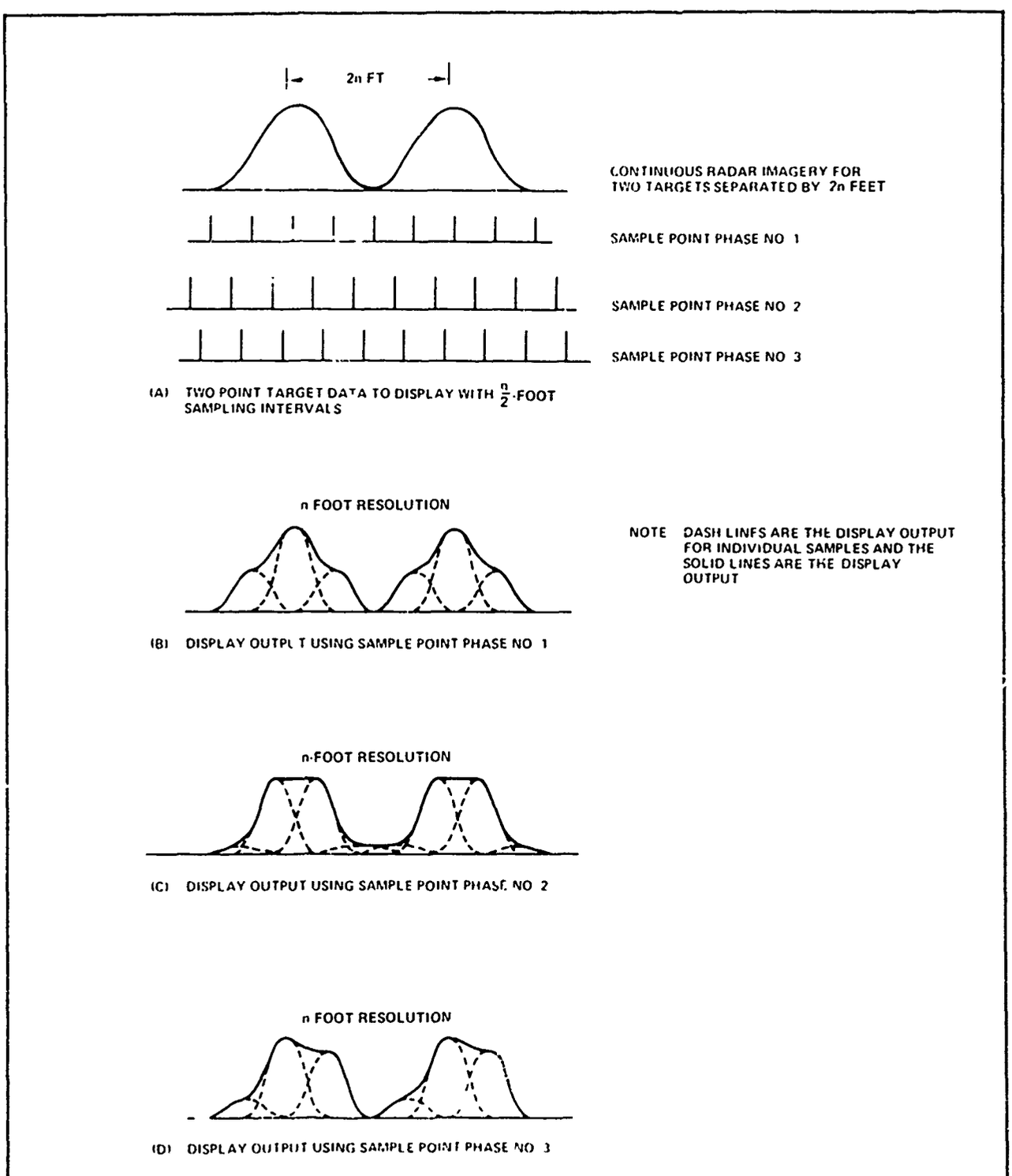

Figure A-2 - Display Response for Two Targets Separated by 2n Feet with Display Samples Taken Every n/2 Feet

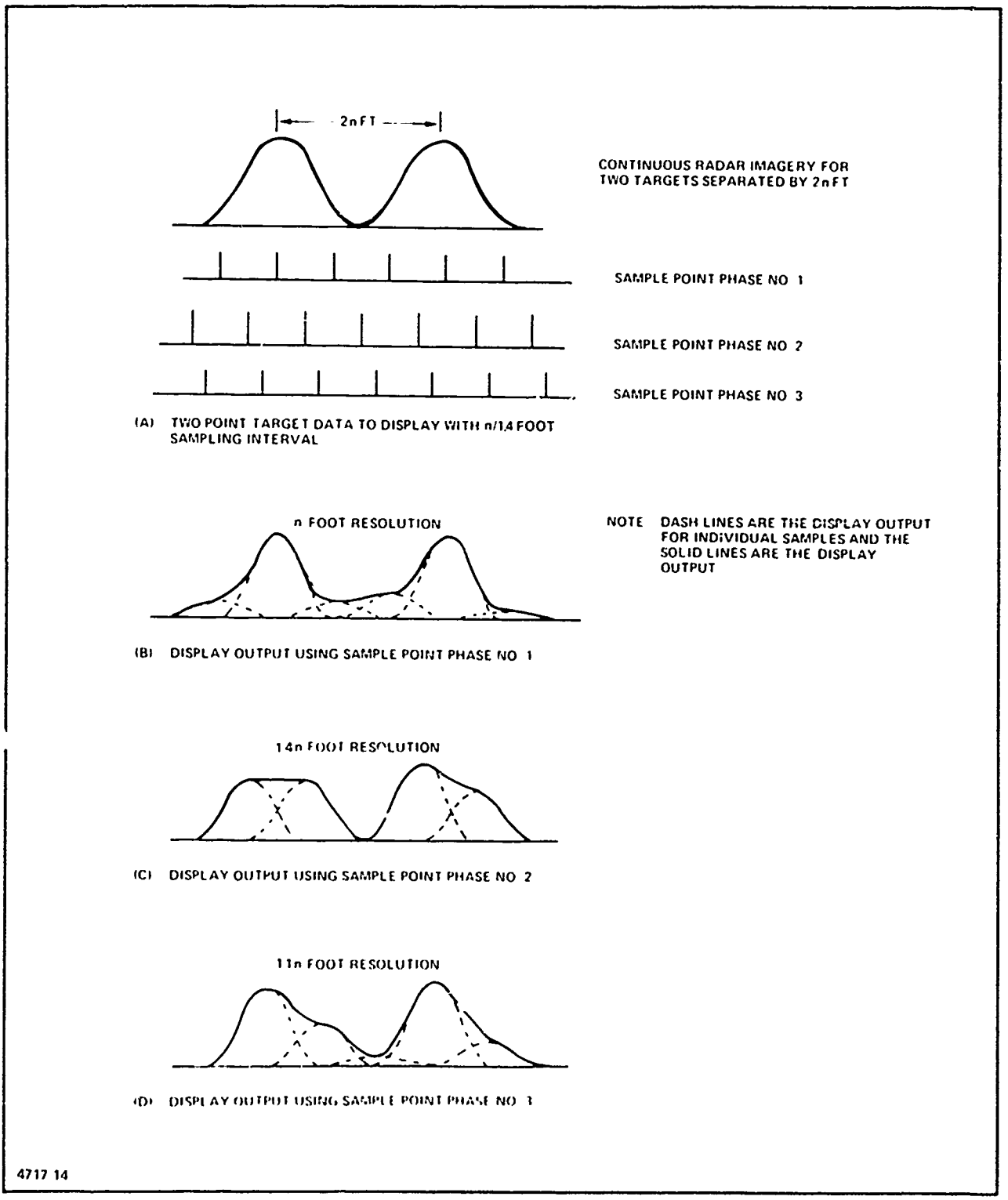

Figure A-3 - Display Response for Two Point Targets Separated by 2n Feet with Display Samples Taken Every n/1.4 Feet

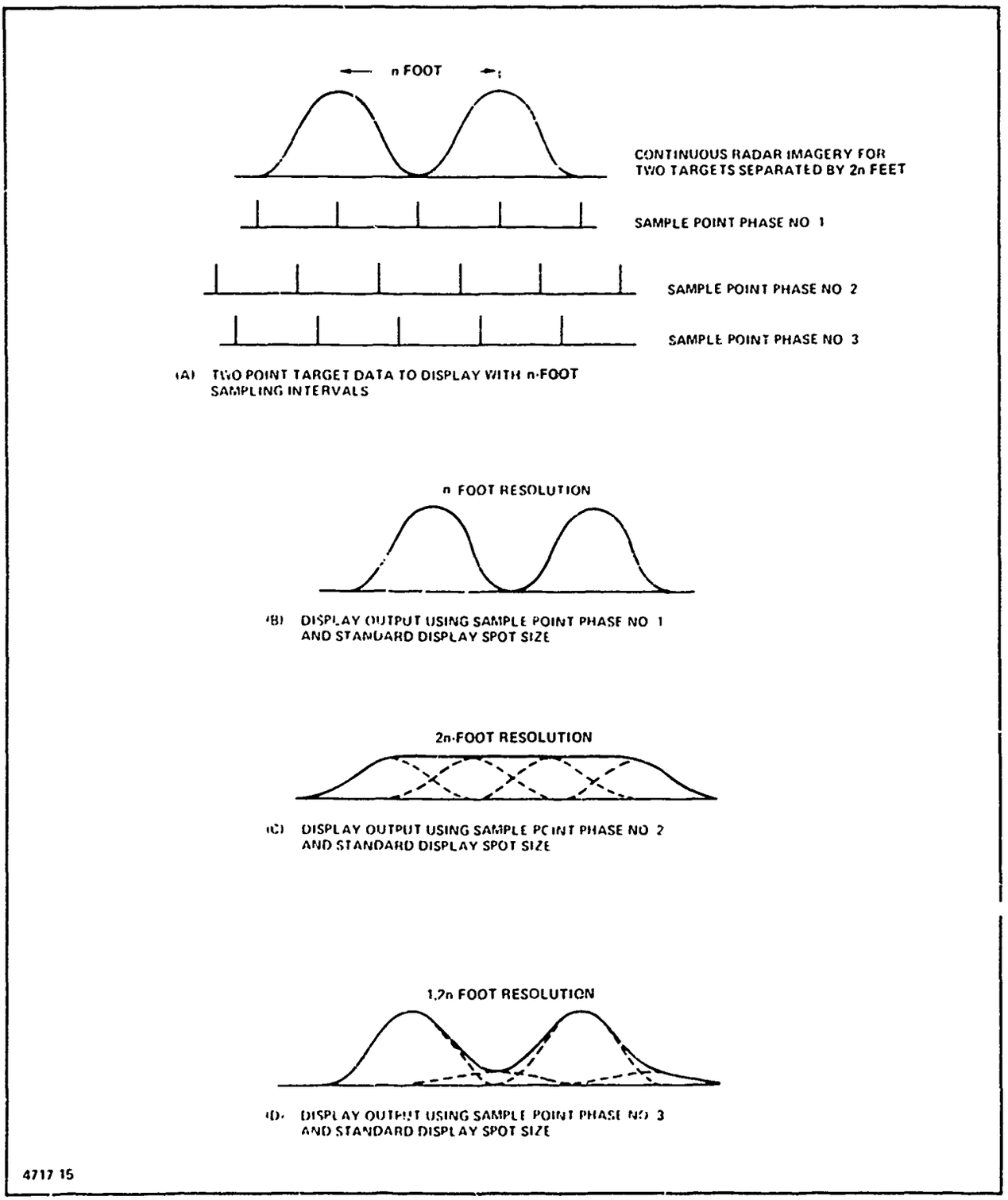

Figure A-4 - Display Response for Two Point Targets Separated by 2n Feet with Display Samples Taken Every n Feet

2. HOW RESAMPLING IS ACCOMPLISHED

Basically, resampling is a method of deriving extra samples by interpolating between adjacent samples. According to Nyquist sampling theorem, a waveform is totally defined if it is sampled at a frequency greater than twice the highest frequency component of the signal. Therefore, if a signal is being sampled at the Nyquist sampling rate, the samples can be operated upon by a digital filter having a bandwidth equal to or greater than the bandwidth of the signal with no effect on the signal.

Nonrecursive digital filters offer the option of having any desired ratio between input and output sampling rates. The output is obtained by convolving the input samples with identically spaced samples of the impulse response of the desired filter. Each time the convolution is performed a new output sample is generated. The convolution can be performed as often as needed to obtain the desired output sampling rate.

For resampling, the desired digital filter has a bandwidth equal to the input signal with uniform amplitude and zero phase. The impulse response of this filter with respect to the input sampling rate is shown in Figure A-5. To double the sampling rate, the filter function is successively shifted one-half sample interval and convolved with corresponding input samples as shown in Figure A-5(B). As can be seen, the shifting can be any amount provided sufficient samples are defined in the reference function. By using the illustrated reference function (sin x/x with nontruncated sidelobes for the above described low-pass filter), exact interpolation can be performed between samples. This exact interpolation does require a fairly large amount of hardware to perform the convolution because it is necessary to multiply many reference functions with the input samples and accumulating the products.

If a slightly degraded response can be tolerated, the digital filter complexity can be significantly reduced by convolving the input with only a few reference samples of the sin x/x reference function. A further simplification can be made if the sampling rate is to be exactly doubled.

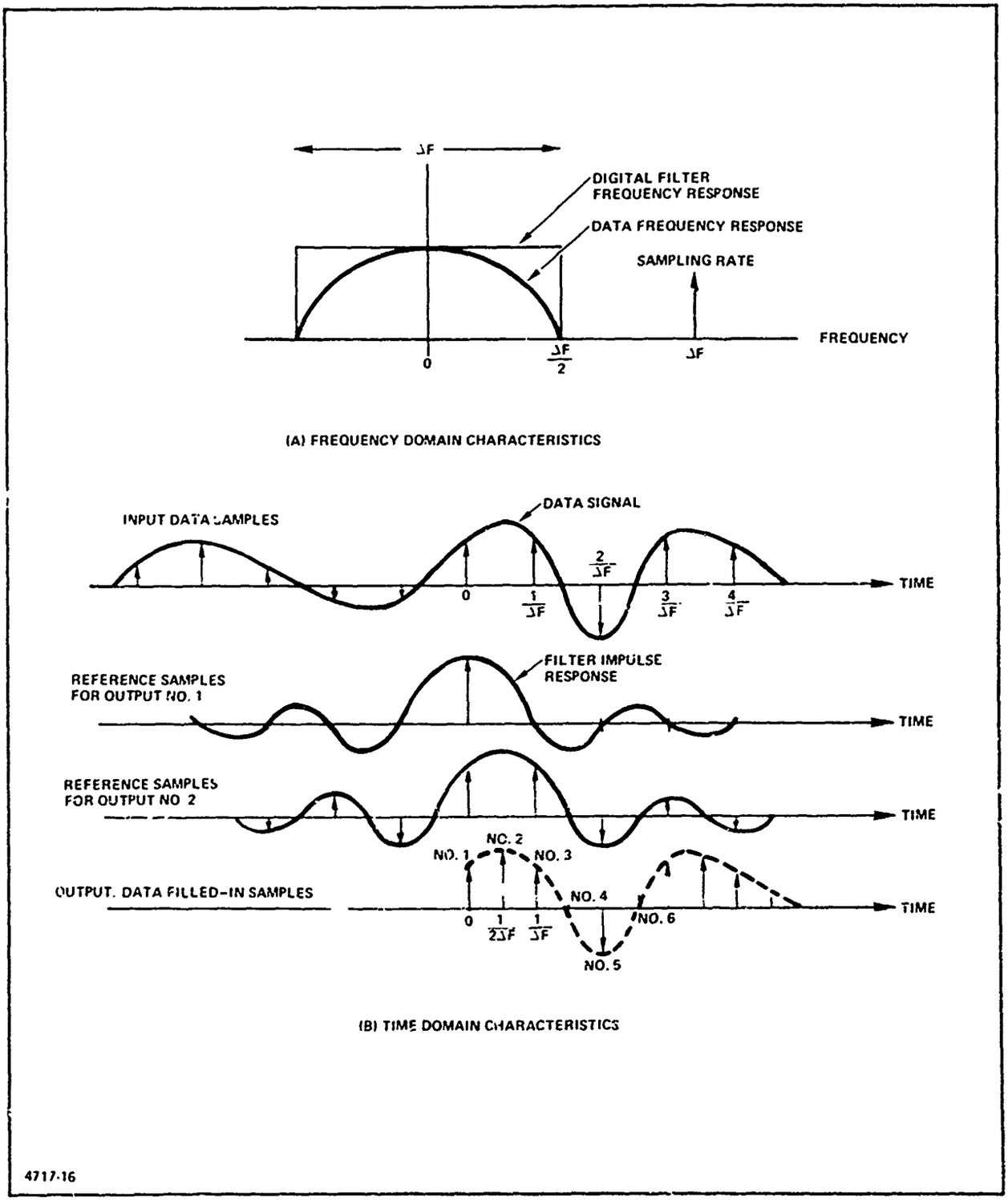

Figure A-5 - Resampling Digital Filter Characteristics

The most direct method of doubling the sampling rate is to generate an extra sample midway between input samples. As can be seen in Figure A-5(B) (reference sample for output no. 1), when an output sample occurring at the same time as the input sample is desired, the reference function samples all become zero except for a single one in the mainlobe having unity amplitude. Convolution with this reference function yields the same result as would be obtained if the input were gated directly to the output. Figure A-6 shows a block diagram of a method of implementing this operation. The output of the first latch is gated directly out through the data select for every other output pulse.

The intermediate sample is obtained by convolving a number of input samples (four in the example of Figure A-6) with corresponding symmetrical reference function samples from the sin x/x reference function. See reference sample for output no. 2 in Figure A-5(B). The convolution is performed by simply multiplying contiguous samples by the appropriate weighting functions and summing the products.

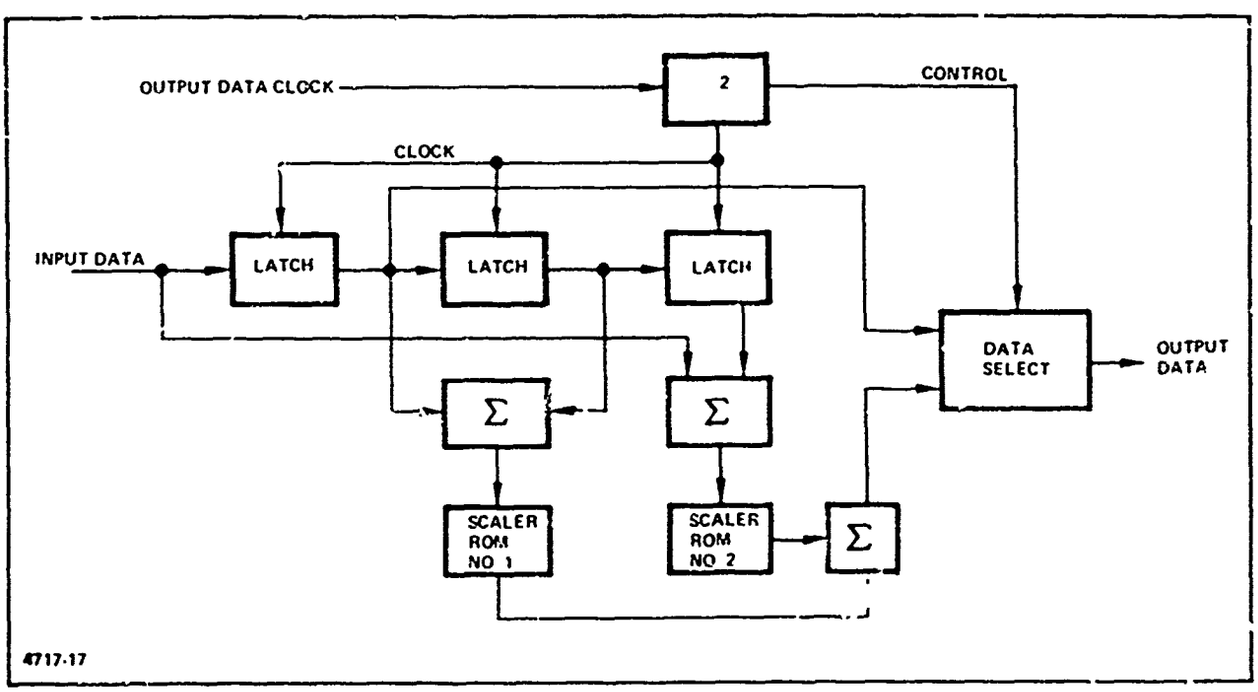

Figure A-6 - Simplified Block Diagram of Resampling

3. RANGE AND AZIMUTH RESAMPLING

The concepts described above can be applied to both range and azimuth resampling. Range samples of radar data occur sequentially in time and can be processed directly, as shown in Figure A-6. Azimuth samples require additional memory to store the range samples associated with each azimuth sample; i.e., an azimuth sample contains a range sample for every range bin being processed. To perform a convolution, at least three contiguous azimuth samples must be stored. To minimize hardware, azimuth resampling is normally performed before range resampling.